FUJITSU SEMICONDUCTOR
DATA SHEET

Prelminary
2004.11.12

32-Bit Proprietary Microcontroller

LSI Network Security System

MB91401

■ DESCRIPTION

The MB91401 is a network security LSI incorporating a Fujitsu's 32-bit, FR-family RISC microcontroller with 10/100Base-T MAC Controller, encryption function and authentication function. The LSI contains an encryption authentication hardware accelerator that boosts the LSI's performance for encryption and authentication communication (IKE/IPsec/SSL) to be demanded further.

The MAC controller has a packet filtering function that reduces the load on the CPU for an increasing amount of packet processing. In addition, the board has the External interface for high-speed data communication with various external hosts, USB ports as general-purpose interfaces, and various card interfaces.

■ FEATURES

• Encryption and authentication processing by hardware accelerator function

The LSI performs processing five times faster than by the conventional combination of encryption/authentication hardware macros and software or about 400 times faster than by software only. In addition, CPU processing load factor to be involved in the encryption and the authentication processing can be decreased to 1/5 or less.
Also, the LSI uses the embedded accelerator to execute that public-key encryption algorithm about 100 times faster than by software processing, which generally puts an extremely heavy load microcontrollers.

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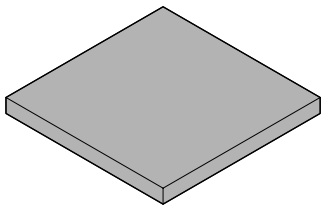
■ PACKAGE

244-pin plastic FBGA



(BGA-240P-M01)

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- For DES-ECB/DES-CBC/3DES-ECB/3DES-CBC mode*
- For MD5/SHA-1/HMAC-MD5/HMAC-SHA-1 mode
- DH group: for 1 (MODP 768 bit) /2 (1024 bit)

For the encryption/authentication macros, a software library is available by contacting the Fujitsu sales representative as required.

* : Encryption function (DES/3DES)
Method to encrypt, and to decrypt plaintext in 64 bits with code and decoding key to 56 bits. (3DES is repeated three times. The key can be set by 168 bits or less.)

• Packet filtering function

The internal feature for L3/L4 packet filtering lets specific data pass or halts them based on address (IP/MAC address) settings. Moreover, the function (multicast address filter function) to receive the data is provided in case of the multicast address registered besides my address, too.

- IEEE 802.3 compliant 10/100M MAC
- MII interface (for full-duplex/half-duplex)
- SMI interface for PHY device control

Note : The filtering function of layer 3/4 (mount on hardware).
This feature determines whether to pass or discard packets when this layer 3 (network layer) IP addresses or layer 4 (transport layer) TCP/UDP port numbers match conditions.

• Outside interface with telecommunication facility (EXTERNAL INTERFACE)

MB91401 is equipped it with the register for the communication and with mass sending and receiving FIFO that achieves a large amount of data sending and receiving. Host functions include processing of data stored in a 3 KByte receive buffer and a 1.5 KByte transmit buffer and stopping of data reception. when the buffers become full.
This enables communication control even during data transmission and reception, thereby improving communication efficiency while reducing the CPU load.

- 8/16 bit data port
- Equipped with sending and receiving data port control function
- Transfer rate : 133 Mbps (Max)

• General Purpose IO (GPIO)

The interruption can be generated in the I/O port in eight bits according to changing the input signal. Moreover, the I/O setting can be done in each bit.

• Memory Interface

It is possible to connect it with an external memory.

• USB Function Controller

It can not operate as host USB.

- For USB FUNCTION Rev2.0FS
- Double Buffer Specification

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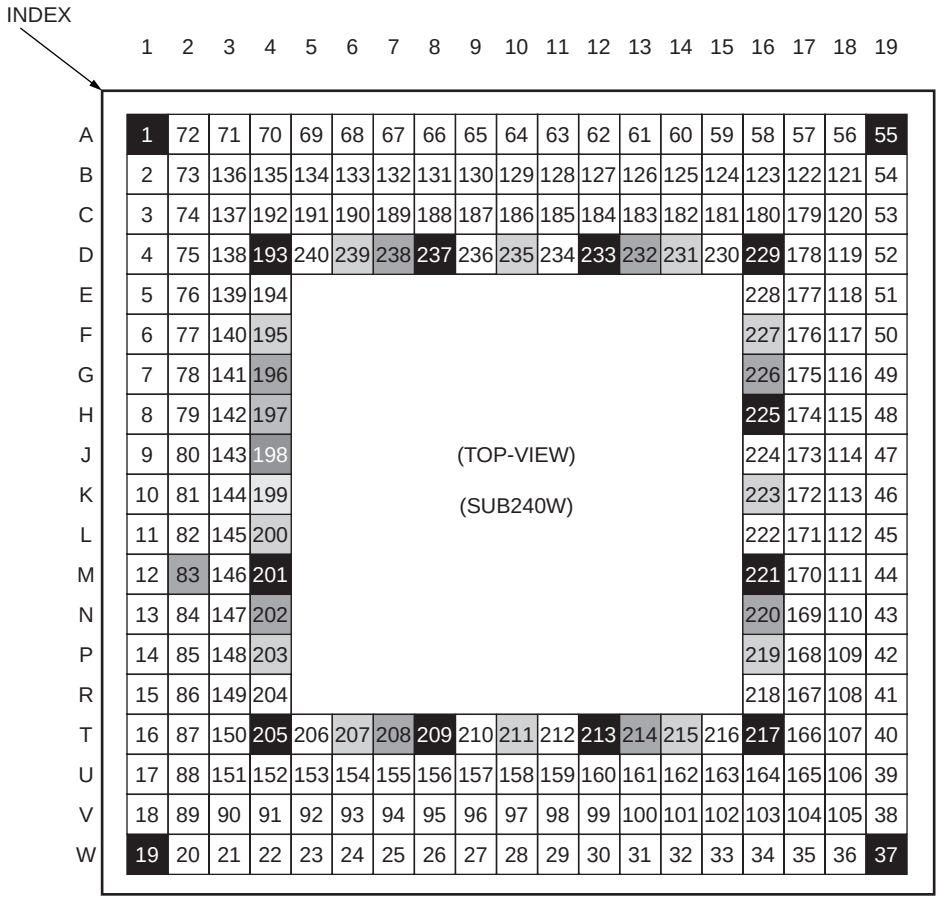
- **CARD Interface (CompactFlash)**

  The CompactFlash interface is a memory and I/O mode correspondence. It corresponds to the I/O of data such as not only the memory card but also the communication cards.

- **I²C Interface**
  - Master/slave sending and receiving
  - For standard mode (100 Kbps Max)

■ PIN ASSIGNMENT



: signal (204 lines)

: PLLVDD (1 line) 199

: PLLVSS (1 line) 197

: VDDI (12 lines) 195, 200, 203, 207, 211, 215, 1219, 223
227, 231, 235, 239

: VDDE (9 lines) 83, 196, 202, 208, 214, 220, 226, 232, 238

: VSS (16lins) 1, 19, 37, 55, 193, 198, 201, 205, 209
213, 217, 225, 229, 233, 237

■ PIN NUMBER TABLE

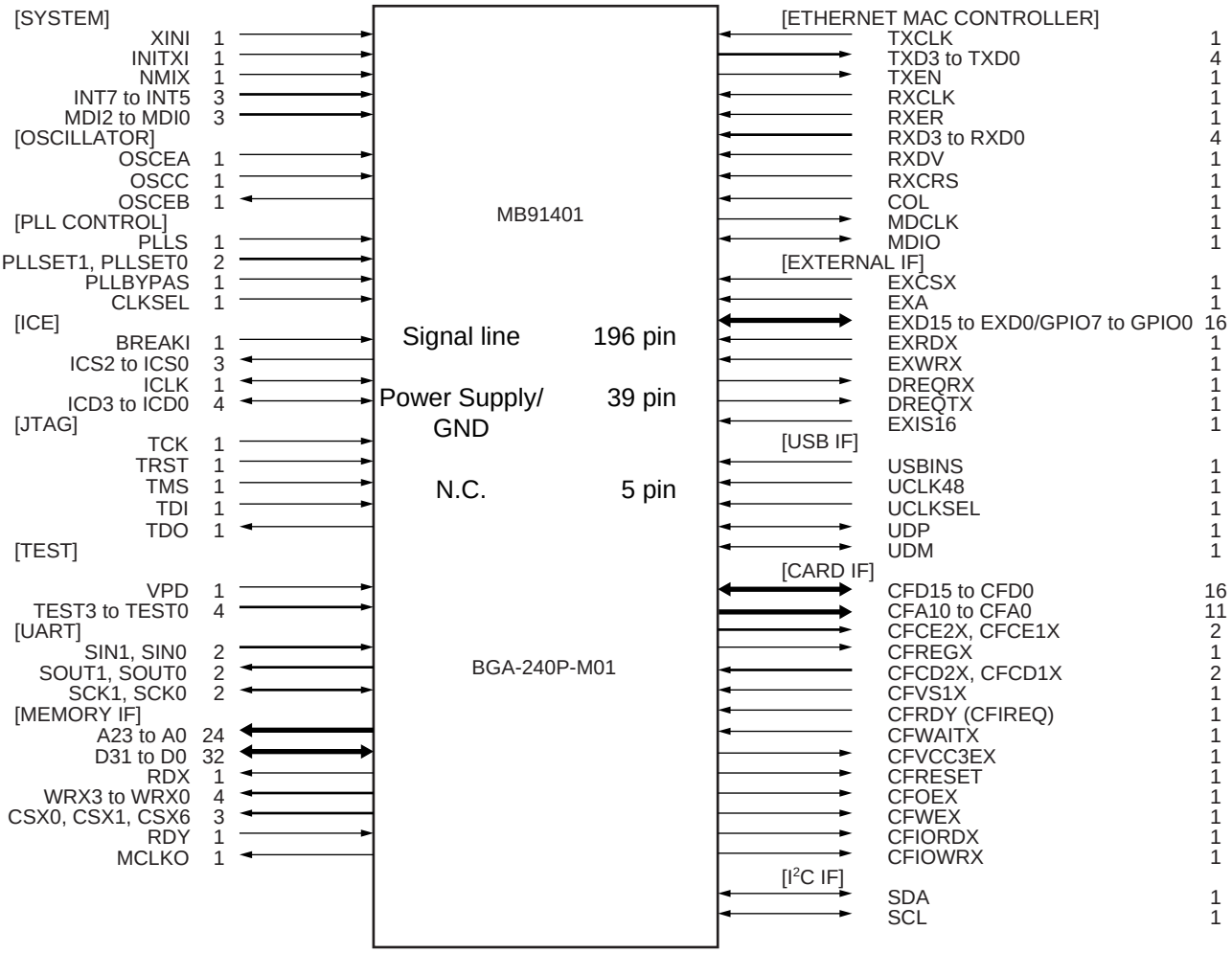
Pin Number	Pin name
1	VSS
2	CFD15
3	ICLK
4	ICS0
5	TDI
6	UCLK48
7	TMS
8	XINI
9	PLLBYPAS
10	OSCEB
11	TEST0
12	OSCEA
13	TEST2
14	SCK0
15	SIN0
16	INT5
17	A3
18	A2
19	VSS
20	A4
21	A7
22	A10
23	A13
24	A16
25	MCLKO
26	A21
27	RDX
28	WRX2
29	CSX0
30	N.C.
31	D0
32	D2
33	D5
34	D9
35	D12
36	D15
37	VSS
38	D17
39	D18
40	D20
41	D23
42	D27
43	TXEN
44	TXD0
45	RXD0
46	TXCLK
47	RXD2
48	RXCLK
49	EXIS16
50	EXCSX
51	EXD0/GPIO0
52	EXD4/GPIO4
53	EXD7/GPIO7
54	EXD10
55	VSS
56	EXD12
57	EXD13
58	CFCD1X
59	SCL
60	CFRDY

Pin Number	Pin name
61	UDP
62	CFWEX
63	CFCE1X
64	CFIORDX
65	CFA1
66	CFA5
67	CFA8
68	CFD0
69	CFD3
70	CFD7
71	CFD10
72	CFD13
73	CFD14
74	ICS2
75	ICS1
76	BREAKI
77	CLKSEL
78	TRST
79	MDI0
80	MDI2
81	PLLSET0
82	TEST1
83	VDDE
84	TEST3
85	SIN1
86	SOUT0
87	INT6
88	A6
89	A5
90	A8
91	A11
92	A14
93	A17
94	A19
95	A22
96	WRX3
97	WRX1
98	CSX1
99	N.C.
100	D1
101	D3
102	D6
103	D10
104	D13
105	D16
106	D19
107	D21
108	D24
109	D28
110	D30
111	TXD1
112	RXD1
113	RXER
114	RXD3
115	RXCRS
116	EXA
117	EXRDX
118	EXD1/GPIO1
119	EXD5/GPIO5
120	EXD8

Pin Number	Pin name
121	EXD11
122	EXD14
123	CFCD2X
124	UCLKSEL
125	CFWAITX
126	N.C.
127	CFOEX
128	CFCE2X
129	CFIOWRX
130	CFA2
131	CFA6
132	CFA9
133	CFD1
134	CFD4
135	CFD8
136	CFD11
137	CFD12
138	ICD0
139	ICD1
140	ICD3
141	TDO
142	MDI1
143	VPD
144	PLLSET1
145	OSCC
146	TCK
147	PLLS
148	SCK1
149	SOUT1
150	INT7
151	A9
152	A12
153	A15
154	A18
155	A20
156	A23
157	RDY
158	WRX0
159	CSX6
160	N.C.
161	N.C.
162	D4
163	D7
164	D11
165	D14
166	D22
167	D25
168	D29
169	D31
170	TXD2
171	TXD3
172	RXDV
173	COL
174	DREQRX
175	DREQTX
176	EXWRX
177	EXD2/GPIO2
178	EXD6/GPIO6
179	EXD9
180	EXD15

Pin Number	Pin name
181	SDA
182	USBINS
183	UDM
184	CFRESET
185	CFREGX
186	CFA0
187	CFA3
188	CFA7
189	CFA10
190	CFD2
191	CFD5
192	CFD9
193	VSS
194	ICD2
195	VDDI
196	VDDE
197	PLLVSS
198	VSS
199	PLLVDD
200	VDDI
201	VSS
202	VDDE
203	VDDI
204	INITXI
205	VSS
206	NMIX
207	VDDI
208	VDDE
209	VSS
210	A0
211	VDDI
212	A1
213	VSS
214	VDDE
215	VDDI
216	D8
217	VSS
218	D26
219	VDDI
220	VDDE
221	VSS
222	MDCLK
223	VDDI
224	MDIO
225	VSS
226	VDDE
227	VDDI
228	EXD3/GPIO3
229	VSS
230	CFVS1X
231	VDDI
232	VDDE
233	VSS
234	CFVCC3EX
235	VDDI
236	CFA4
237	VSS
238	VDDE
239	VDDI
240	CFD6

■ PIN DESCRIPTION



SYSTEM (9 pin)

Pin name	Pin no.	Polarity	I/O	Circuit	Function/application
XINI	8	—	IN	D	Clock input pin Input pin of clock generated in clock generator. 10 MHz to 50 MHz frequency can be input.
INITXI	204	Nega-tive	IN	D	Reset input pin This pin inputs a signal to initialize the LSI. When turning on the power supply, apply “0” to the pin until the clock signal input to the CLKIN pin becomes stable. All built-in registers and external pins are initialized, and the built-in PLL is stopped when “0” is asserted to INITXI.
NMIX	206	Nega-tive	IN	D	NMI input pin Non-Maskable Interrupt signal
INT7 INT6 INT5	150 87 16	—	IN	D	External interrupt input pins These pins input an external interrupt request signal. For external interrupt detection, set the ENIR, EIRR and ELVR registers of the FR core.
MDI2 MDI1 MDI0	80 142 79	—	IN	D	Mode pins These pins determine the operation mode of the LSI. Always set this bit to “001”.

OSCILLATOR (3 pin)

Pin name	Pin no.	Polarity	I/O	Circuit	Function/application
OSCEA	12	—	IN	G	Crystal oscillation input pin Input pin of crystal oscillation cell.
OSCC	145	Nega-tive	IN	D	Crystal oscillation control input pin Oscillation control pin of crystal oscillation cell. “0” : Oscillation “1” : Oscillation stop
OSCEB	10	—	OUT	G	Crystal oscillation output pin Output pin of crystal oscillation cell.

PLL CONTROL (5 pin)

Pin name	Pin no.	Polarity	I/O	Circuit	Function/application
PLLS	147	—	IN	D	PLL/through mode (reset) switching input pin “0” : PLL through mode (oscillation stop) “1” : PLL oscillation mode
PLLSET1	144	—	IN	D	Input clock division ratio select input pin “0” : Input clock direct “1” : Input clock divided by 2
PLLSET0	81	—	IN	D	Division ratio select input to PLL FB pin “0” : Two dividing frequency is input to the terminal FB. “1” : Four dividing frequency is input to the terminal FB.
PLLBYPAS	9	—	IN	D	PLL bypass select input pin “0” : PLL used “1” : PLL unused
CLKSEL	77	—	IN	D	Input clock switching input pin “0” : XINI (External clock) “1” : Built-in OSC generating clock

ICE (9 pin)

Pin name	Pin no.	Polarity	I/O	Circuit	Function/application
BREAKI	76	—	IN	D	Emulator break request pin This pin inputs the emulator break request when an ICE is connected.
ICS2 ICS1 ICS0	74 75 4	—	OUT	F	Emulator chip status pins These pins output the emulator status when an ICE is connected.
ICLK	3	—	I/O	B	Emulator clock pin This pin serves as the emulator clock pin when an ICE is connected.
ICD3 ICD2 ICD1 ICD0	140 194 139 138	—	I/O	B	Emulator data pins These pins serve as the emulator data bus when an ICE is connected.

JTAG (5 pin)

Pin name	Pin no.	Polarity	I/O	Circuit	Function/application
TCK	146	—	IN	E	JTAG test clock pin Note : Please input “1” when unused.
TRST	78	—	IN	E	JTAG test reset pin Note : Please input “0” when unused.
TMS	7	—	IN	E	TAP controller mode select pin Note : Please input “1” when unused.
TDI	5	—	IN	E	JTAG test data input pin JTAG test serial data input pin. Note : Please input “1” when unused.
TDO	141	—	OUT	F	JTAG test data output pin JTAG test serial data output pin

TEST (5 pin)

Pin name	Pin no.	Polarity	I/O	Circuit	Function/application
VPD	143	—	IN	—	Mode pin Input “0” to this pin.
TEST3 TEST2 TEST1 TEST0	84 13 82 11	—	IN	D	Test pin Input “0000” to this pin. Note : Don’t set other than above description.

UART (6 pin)

Pin name	Pin no.	Polarity	I/O	Circuit	Function/application
SIN1 SIN0	85 15	—	IN	D	Serial data input pins Serial data input pin of UART built-in FR core.
SOUT1 SOUT0	149 86	—	OUT	F	Serial data output pins Serial data output pin of UART built-in FR core.
SCK1 SCK0	148 14	—	I/O	B	Serial clock I/O pins Serial clock input/output pin of UART built-in FR core.

MEMORY IF (66 pin)

Pin name	Pin no.	Polarity	I/O	Circuit	Function/application
A23 A22 A21 A20 A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	156 95 26 155 94 154 93 24 153 92 23 152 91 22 151 90 21 88 89 20 17 18 212 210	—	OUT	B	Address output pins 24 bits address signal pin.

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Pin name	Pin no.	Polarity	I/O	Circuit	Function/application
D31 D30 D29 D28 D27 D26 D25 D24 D23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	169 110 168 109 42 218 167 108 41 166 107 40 106 39 38 105 36 165 104 35 164 103 34 216 163 102 33 162 101 32 100 31	—	I/O	B	Data input/output pins 32 bits data input/output signal pin.
CSX6 CSX1 CSX0	159 98 29	Negative	OUT	B	Chip select output pins 3-bit chip select signal pin. Output the “L” level when accessing to external memory.
RDX	27	Negative	OUT	B	Read strobe output pin Read strobing signal pin. Output the “L” level when read accessing.
WRX3 WRX2 WRX1 WRX0	96 28 97 158	Negative	OUT	B	Write strobing output pins Write strobing signal pin. Output the “L” level when write accessing.
MCLKO	25	—	OUT	F	Memory clock output pin Clock for peripheral resources pin.
RDY	157	Positive	IN	D	External RDY input pin When the external bus is not completed, the bus cycle can be extended by inputting “0”.

ETHERNET MAC CONTROLLER (17 pin)

Pin name	Pin no.	Polarity	I/O	Circuit	Function/application
RXCLK	48	—	IN	D	Clock input for reception pin MII sync signal during reception. The frequency is 2.5 MHz at 10 Mbps and 25 MHz at 100 Mbps.
RXER	113	Positive	IN	D	Receive error input pin It is recognized that there is an error in the reception packet when “1” is input from the PHY device at receiving.
RXDV	172	Positive	IN	D	Receive data valid input pin It is recognized that receive data is effective.
RXCRS	115	Positive	IN	D	Career sense input pin The state that the reception or the transmission is done is recognized.
RXD3 RXD2 RXD1 RXD0	114 47 112 45	—	IN	D	Receive data input pins 4-bit data input from PHY device.
COL	173	Positive	IN	D	Collision detection input pin When TXEN signal is active and “1”, the collision is recognized. The collision is not recognized without these conditions.
TXCLK	46	—	IN	D	Clock input for transfer pin It becomes synchronous of MII when transmitting. The frequency is 2.5 MHz at 10 Mbps and 25 MHz at 100 Mbps.
TXEN	43	Positive	OUT	F	Transfer enable output pin It is shown that effective data is on the TXD bus. It is output synchronizing with TXCLK.
TXD3 TXD2 TXD1 TXD0	171 170 111 44	—	OUT	F	Transfer data output pins 4-bit data bus sent to the PHY device. It is output synchronizing with TXCLK.
MDCLK	222	—	OUT	F	SMI clock output pin SMI IF clock pin Connect to SMI clock input pin of PHY device.
MDIO	224	—	I/O	B	SMI data input/output pin Connect to SMI data of PHY device.

EXTERNAL IF (23 pin)

Pin name	Pin no.	Polarity	I/O	Circuit	Function/application
EXCSX	50	Nega-tive	IN	D	External chip select input pin Chip select input pin from external host.
EXA	116	—	IN	D	External address input pin Address input pin from external host. “0” : Register select “1” : FIFO data select
EXD15 EXD14 EXD13 EXD12 EXD11 EXD10 EXD9 EXD8	180 122 57 56 121 54 179 120	—	I/O	B	External data input/output pins The I/O terminal of data bus bit of bit15 to bit8 with an external host.
EXD7/GPIO7 EXD6/GPIO6 EXD5/GPIO5 EXD4/GPIO4 EXD3/GPIO3 EXD2/GPIO2 EXD1/GPIO1 EXD0/GPIO0	53 178 119 52 228 177 118 51	—	I/O	B	External data/GPIO input/output pins The I/O terminal of data bus bit of bit7 to bit0 with an external host. Note : When EXIS16 “0” input, it becomes the I/O terminal of GPIO7 to GPIO0.
EXRDX	117	Nega-tive	IN	D	External read strobing input pin Read strove input pin from external host
EXWRX	176	Nega-tive	IN	D	External write strobing input pin Write strove input pin from external host
EXIS16	49	—	IN	D	External data bus width select input pin Bit width select pin of EXD “0” : 8 bit (Note : EXD15 to EXD8 are enabled.) “1” : 16 bit
DREQRX	174	Nega-tive	OUT	F	External reception data request output pin Recordable data to reception FIFO is shown.
DREQTX	175	Nega-tive	OUT	F	External transfer data request output pin It is shown that there are data in transmission register and transmission FIFO.

USB IF (5 pin)

Pin name	Pin no.	Polarity	I/O	Circuit	Function/application
UDP	61	—	I/O	C	USB data D + (differential) pin I/O signal pin on the plus side of the USB data. Use the LSI with 25 Ω to 30 Ω (27 Ω recommended) external series load resistors, 1.5 kΩ pull-up resistors and about 100 kΩ resistors. Input “0” when the USB macro is unused.
UDM	183	—	I/O	C	USB data D − (differential) pin I/O signal pin on the minus side of the USB data. Use the LSI with 25 Ω to 30 Ω (27 Ω recommended) external series load resistors, 1.5 kΩ pull-up resistors and about 100 kΩ resistors. Input “0” when the USB macro is unused.
USBINS	182	—	IN	D	USB insert input pin USB socket input detection pin. Be sure to input “0” when not using USB macro.
UCLK48	6	—	IN	D	48 MHz input (external clock input) pin This pin inputs an external 48-MHz clock signal. The USB macro operates based on this clock. Input the clock with high accuracy (as not only LSI but also a device) more than 2500 ppm. Input “0” when the USB macro is unused.
UCLKSEL	124	—	IN	D	USB clock select pin Clock select pin using for USB macro “0” : Using internal clock “1” : Using UCLK48

CARD IF (41 pin)

Pin name	Pin no.	Polarity	I/O	Circuit	Function/application
CFD15 CFD14 CFD13 CFD12 CFD11 CFD10 CFD9 CFD8 CFD7 CFD6 CFD5 CFD4 CFD3 CFD2 CFD0 CFD0	2 73 72 137 136 71 192 135 70 240 191 134 69 190 133 68	—	I/O	B	CF data input/output pins I/O data/status/command signal pin to CompactFlash card side
CFA10 CFA9 CFA8 CFA7 CFA6 CFA5 CFA4 CFA3 CFA2 CFA1 CFA0	189 132 67 188 131 66 236 187 130 65 186	—	OUT	B	CF address 10 to 0 output pins Address output CFA10 to CFA0 pins to CompactFlash card side
CFCE2X	128	Negative	OUT	B	CF card enable output pin Byte access output pin to CompactFlash card side Note : Supported for access to CFD7 to CFD0. When “L” level is output, odd number byte access of the word is shown.
CFCE1X	63	Negative	OUT	B	CF card enable output pin Byte access output pin to CompactFlash card side Note : Supported for access to CFD7 to CFD0. When “L” level is output at word access, even number byte access of the word is shown. When the byte is accessed, the even number byte and odd number byte access become possible because CFA0 and CFCE2X are combined and used by it.
CFREGX	185	Negative	OUT	B	CF Attribute/Common switching output pin Attribute/Common switching output pin to CompactFlash card side “H” : Common Memory select “L” : Attribute Memory select
CFCD2X	123	Negative	IN	E	Card connection detect input pin : CFCD2X Checking connection pin of the socket and CompactFlash card. It is shown that the CompactFlash card was connected when this signal and CFCD1X are both input by “0”.

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Pin name	Pin no.	Polarity	I/O	Circuit	Function/application
CFCD1X	58	Nega-tive	IN	E	Card connection detect input pin : CFCD1X Checking connection pin of the socket and CompactFlash card. It is shown that the CompactFlash card was connected when this signal and CFCD2X are both input by “0”.
CFVS1X	230	Nega-tive	IN	E	CF side GND input pin GND level detection pin from CompactFlash side. The “0” input to the pin assumes that the CompactFlash card can operate at 3.3 V, setting the CFVCC3EX pin to the “L” level.
CFRDY (CFIREQ)	60	Posi-tive (Nega-tive)	IN	E	CF ready input pin : memory card Ready input pin from CompactFlash memory card side “1” : Ready “0” : Busy (CF interrupt : I/O card) Interrupt request pin of CompactFlash I/O card. It is shown the interrupt request was done from the I/O card when input to this signal by “0”.
CFWAITX	125	Nega-tive	IN	E	Cycle wait input pin during CF execution Cycle wait input pin from CompactFlash card side “0” : It is shown that there is a wait demand at the cycle under execution. “1” : It is shown that there is no wait demand at the cycle under execution.
CFVCC3EX	234	Nega-tive	OUT	B	CF3.3 V power enable output pin Outputs “L” level when the CompactFlash card is operable at 3.3 V. The output signal enables 3.3-volt power supply to the CompactFlash card. The pin outputs “L” level only when the CFVS1X pin detects “0”; otherwise, the pin outputs “H”.
CFRESET	184	Posi-tive	OUT	A	CF reset output pin Reset output pin to CompactFlash card side. CompactFlash is reset at “H” output.
CFOEX	127	Nega-tive	OUT	B	CF read strobe output pin Read strove output pin to CompactFlash card (memory mode and Attribute memory area)
CFWEX	62	Nega-tive	OUT	B	CF register write output pin Write clock output pin to CompactFlash card (register write and Card Configuration Register area). The register write is executed at the rising edge from “L” to “H”.
CFIORDX	64	Nega-tive	OUT	B	CFIO read strobing output pin Read strove output pin to CompactFlash card (I/O mode)
CFIOWRX	129	Nega-tive	OUT	B	CFIO write strobing output pin Write strove output pin to CompactFlash card (I/O mode)

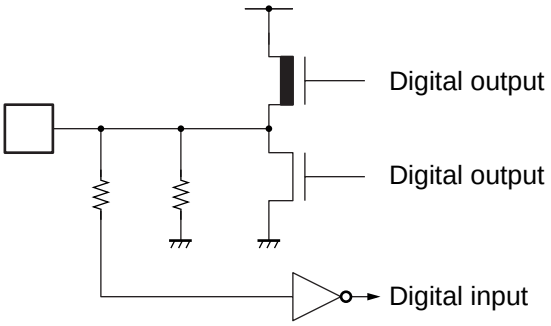
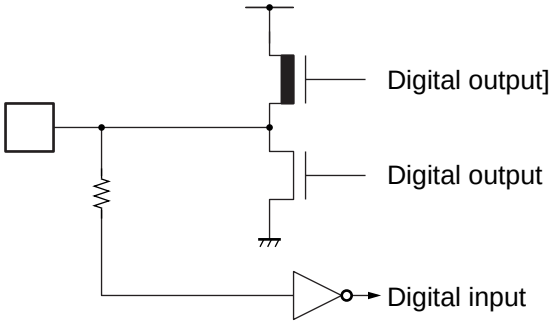
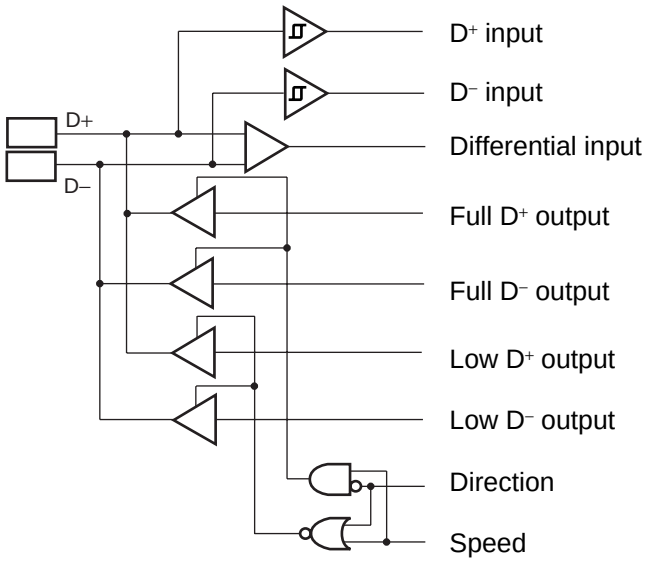
I²C IF (2 pin)

Pin name	Pin no.	Polarity	I/O	Circuit	Function/application
SDA	181	—	I/O	B	Serial data line input/output pin I²C bus data I/O pin
SCL	59	—	I/O	B	Serial clock line input/output pin I²C bus clock I/O pin

Power Supply/GND (39 pin)

Pin name	Pin no.	Polarity	I/O	Circuit	Function/application
PLLVDD	199	—	Power supply	V-E	APLL dedicated power supply pin This pin is for 1.8 V power supply pin.
PLLVSS	197	—	GND	V-S	APLL dedicated GND Pin
VDDE	83 196 202 208 214 220 226 232 238	—	Power supply	V-E	3.3 V power supply pin
VDDI	195 200 203 207 211 215 219 223 227 231 235 239	—	Power supply	V-E	1.8 V power supply pin
VSS	1 19 37 55 193 198 201 205 209 213 217 221 225 229 233 237	—	GND	V-S	GND Pin

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• With pull/down • CMOS level output • CMOS level input • Value of pull-down resistance = approx. 33 kΩ (Typ)
B		• CMOS level output • CMOS level input
C		USB I/O

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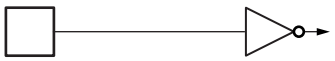
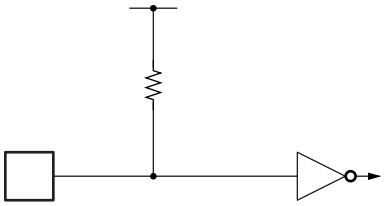
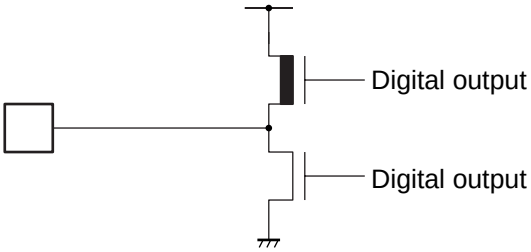
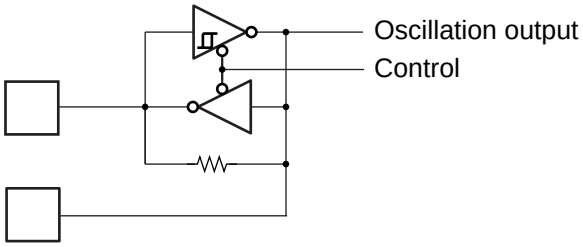
(Continued)

Type	Circuit	Remarks
D		CMOS level input
E		• With pull-up • CMOS level input • Value of pull-up resistance = approx. 33 kΩ (Typ)
F		CMOS level output
G		Oscillation circuit

■ HANDLING DEVICES

Preventing Latch-up

When a voltage that is higher than V_{DDE} and a voltage that is lower than V_{SS} are impressed to the input terminal and the output terminal in CMOS IC or the voltage that exceeds ratings between V_{DDE} to V_{SS} is impressed, the latch-up phenomenon might be caused. If latch-up occurs, the supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Use meticulous care not to let any voltage exceed the maximum rating during device operation.

Separation of power supply pattern

Analog PLL (APLL at the following) is installed in this LSI. The power supply for VCO and for digital is separated in LSI so that the oscillation characteristic of APLL may receive the influence of power supply variation.

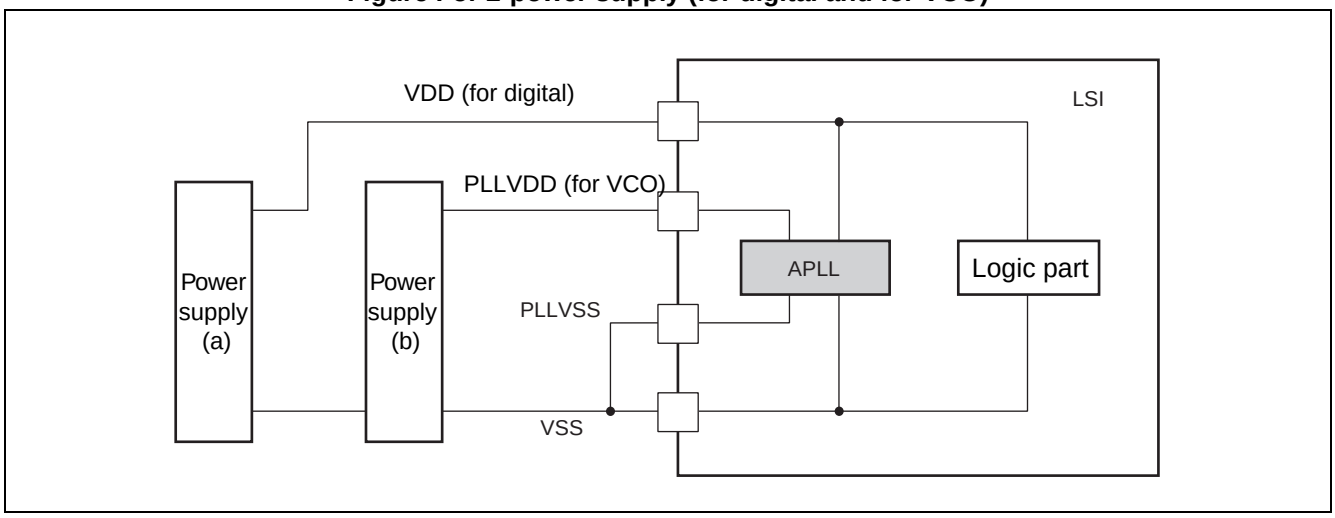
Therefore, the power supply is recommended to be separated also on the mounting base.

• Separation of power supply pattern (recommended)

Take measures to reduce impedance, for example, by using as wide a power pattern as possible.
The recommendation example is shown as follows.

- For two power supplies (for digital and for VCO)
  It is advisable to provide a digital power-supply (a) and VCO power-supply (b) and connect them to the LSI's equivalents, respectively.

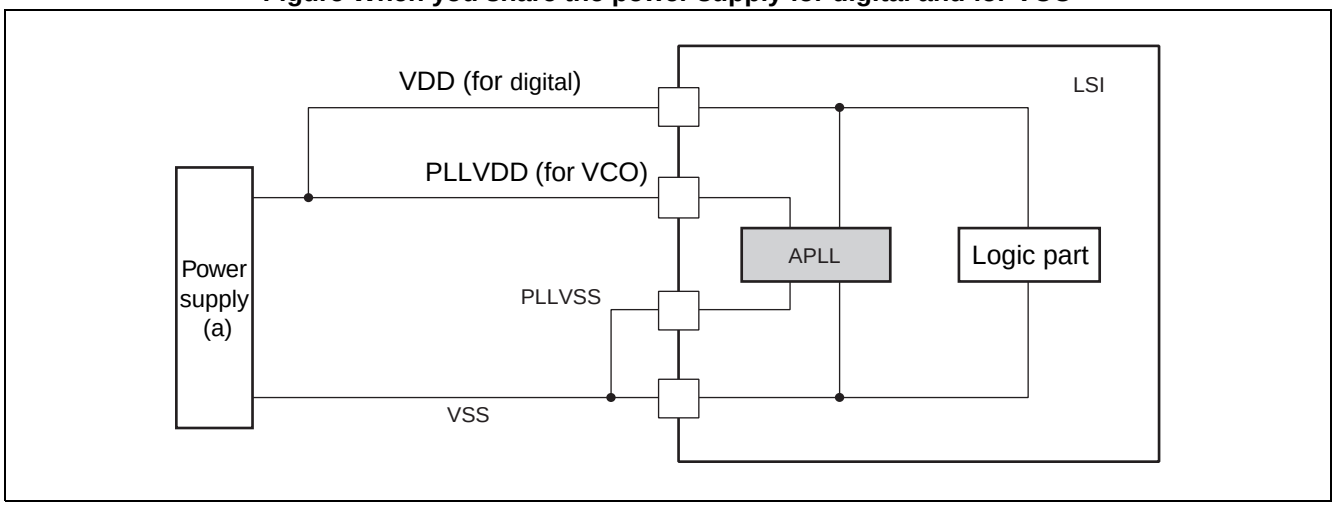
Figure For 2-power supply (for digital and for VCO)



- For the common power supply

To share a single power-supply for digital and VCO uses, it is advisable to separate the output into the digital and VCO wiring patternsand connect them to the LSI.

Figure When you share the power supply for digital and for VCO



Treatment of the unused pins

Leaving unused input pins open results in a malfunction, so process the pull-up or pull-down.

Treatment of OPEN pins

Be sure to use open pins in open state.

Treatment of output pins

A large current may flow to an output pin left connected to the power-supply, another output pin, or to a high capacitance load. Leaving the output pin that way for an extended period of time degrades the device. Use meticulous care in using the device not to exceed the absolute maximum rating.

About Mode (MDI2 to MDI0, VPD) pin and Test (TEST3 to TEST0) pin

Connect these pins directly to VDDE or VSS. To prevent the device from entering test mode accidentally due to noise, minimize the lengths of the patterns between individual mode pins and VDDE or VSS on the PC board as possible and connect them with as low an impedance as possible.

About power supply pins

In products with multiple VDDE, VDDI or VSS pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However you must connect the pins to external power supply and a ground line to lower the electro-magnetic emission level to prevent abnormal operation strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

The power pins should be connected to VDDE, VDDI and VSS of this device at the lowest possible impedance from the current supply source.

It is also advisable to connect a ceramic bypass capacitor of approximately 0.1 μF between VDDE and VSS, and between VDDI and VSS near this device.

Crystal Oscillator Circuit

Noise near the OSCEA terminal may cause the MB91401 to malfunction.

Design the circuit board so that OSCEA terminal, OSCEB terminal and the crystal oscillator, and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended to design the PC board artwork with the OSCEA terminal and OSCEB terminal surrounded by ground plane because stable operation can be expected with such a layout.

■ CONNECTED SPECIFICATION OF MB91401 AND ICE

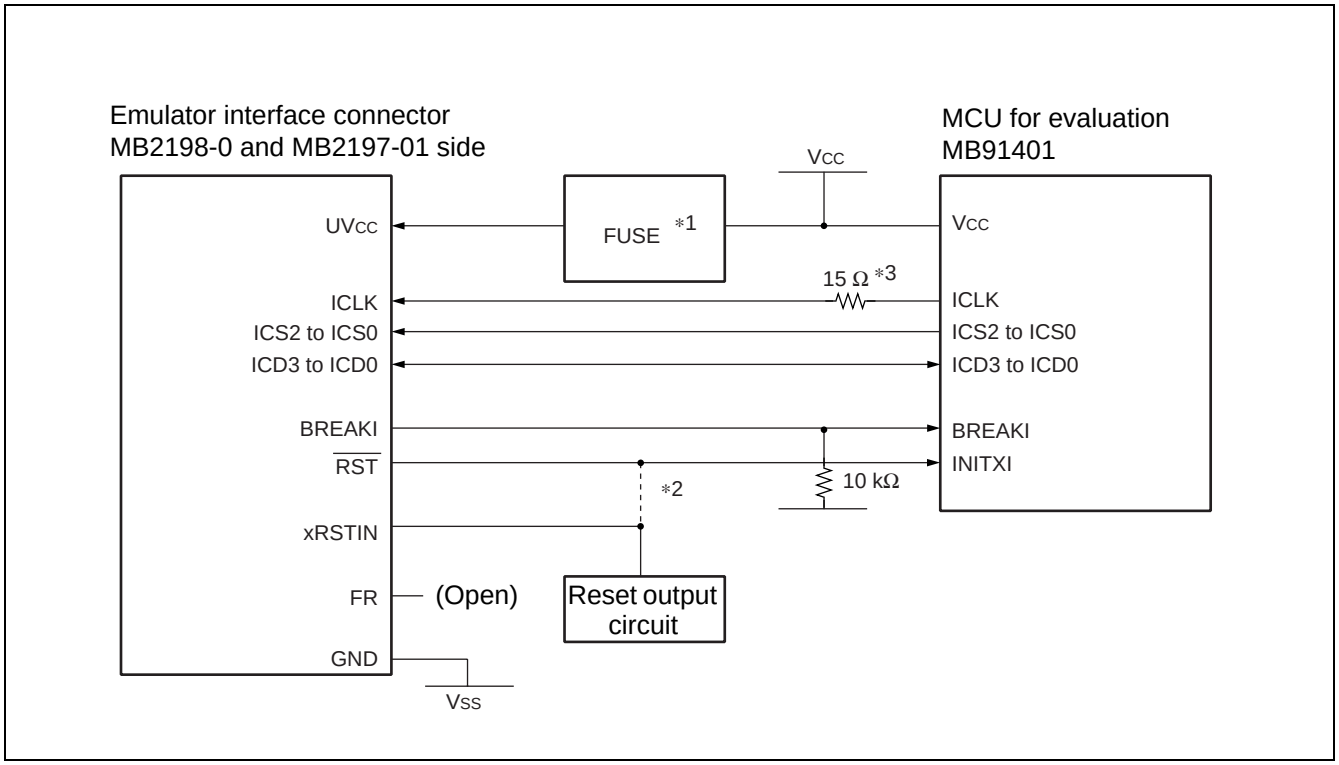
Recommended type and circuit configuration of the emulator interface connector mounting on the user system, attention when designing and wiring regulation are shown.
When the flat cable is used, the combination of the connectors with housing should be selected.

Recommended connector type

Attached cable	Part number	Remarks
FPC cable	FH10A-30S-1SH (Maker : Hirose Electric Co., Ltd.)	With latch

• Circuit composition

Please put the dumping resistance 15 Ω in the series in the ICLK terminal signal because of the stability of operation when connecting it with ICE. Resistance must be mounted near the terminal ICLK of this LSI when you design the printed wiring board.



*1 : Use the line (inter connect) to flow the rating current or more.

*2 : The change circuit might become necessary, and refer to “Precaution when designing”.

*3 : Mount resistance near the terminal ICLK of MB91401.

• Precaution when designing

When evaluation MCU on the user system is operated in the state that the emulator is not connected, should be treated as follow each input terminal of evaluation MCU connected with the emulator interface on the user system.

Therefore, note that the switch circuit etc, might become necessary in the user system when you design.

The terminal processing in each emulator interface is shown as follows.

Pin treatment of emulator interface (DSU-3)

Evaluation MCU terminal name	Pin treatment
RST	To be connected the RST terminal with the reset output circuit in the user system.
Others	To open.

Emulator interface wiring regulations

Signal line name	Wiring regulations
ICLK ICS2 to ICS0 ICD3 to ICD0 BREAKI	• The total wiring length of each signal (From evaluation MCU pin to the emulator interface connector pin) is made within 50 mm. • The difference of the total wiring length of each signal makes within 2 cm and the total wiring length of ICLK is the shortest.
UV_{CC}	• Wire the pattern with capacity more than the ratings current. • Each power supply and GND may cause a short-circuit or reverse connection in between by a wrong connection of a probe. Insert a protection circuit such as a fuse into each power supply pattern to safeguard it.
GND	• Connect directly with a power supply system pattern such as grandopran.

• Reference document

Please match and refer to the following manual for the connection with ICE.

- DSU-FR Emulator MB2198-01 Hardware Manual
- FR20/30 series MB2197-01 Hardware Manual

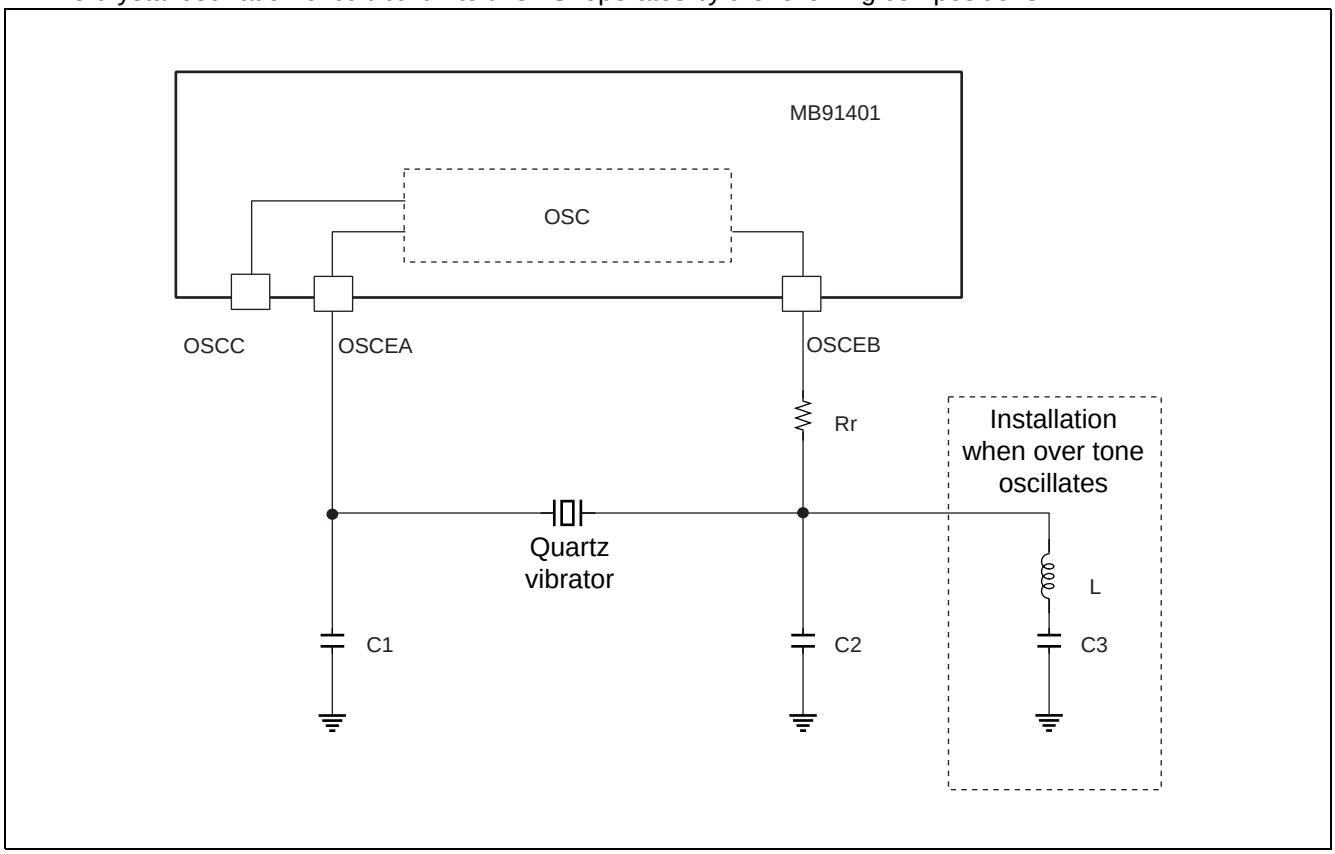
JTAG

The JTAG function is installed in this LSI.

Note that the terminal INITXI should be input in "L" when using JTAG.

Notes when quartz vibrator is mounted

The crystal oscillation circuit built into this LSI operates by the following compositions.



• Pin description

Pin name	Function
OSCC	Oscillation control terminal of crystal oscillation cell (OSC)
OSCEA	Input terminal of crystal oscillation cell (OSC)
OSCEB	Output terminal of crystal oscillation cell (OSC)

When OSCCL is input, the OSCEA and OSCEB oscillate at the natural frequency of the crystal oscillator and propagated into the LSI.

• Circuit constant on external substrate

Circuit constants	Description
C1, C2, C3	External load capacity
L	Inductance
Rr	Dumping resistance (addition if necessary)

- Reference Value

Oscillation frequency	C1, C2	C3	L	Rr
to 30 MHz	5 pF to 33 pF	None	None	None
20 MHz to 50 MHz	5 pF to 15 pF	10 nF approx.	1 µH approx.	None

It is necessary to add C3/L depending on a basic wave and the over tone characteristic of the oscillator of the 20 MHz to 30 MHz belt.

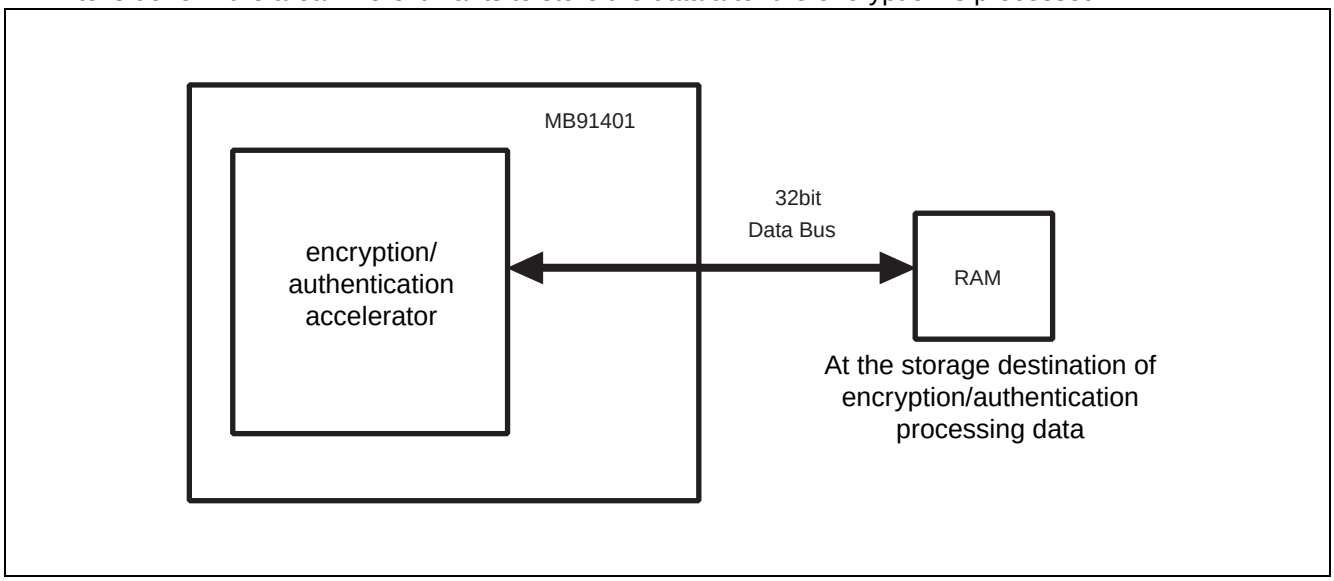
Note : These reference values are standards. The constant changes according to the characteristic of the quartz vibrator used. Therefore, we will recommend the initial evaluation that uses the evaluation sample to the decision of the circuit constant. Please contact FUJITSU representatives about the evaluation sample.

• Notes when encryption/authentication accelarator is used

When using the encryption/authentication installed in this LSI, it is necessary to the following notes.

32-bit data bus

The encryption/authentication accelerator fetches data from the area storing data to be subject to encryption/authentication and encrypts or authenticates the data without CPU intervention. In the encryption processing, write is done in the area where it wants to store the data after the encryption is processed.



Holding request withdrawal demand function OFF

When accessing to the storage destination of encryption/authentication processing data, the encryption/authentication accelerator should hold an internal bus of this LSI.

Therefore, when the encryption/authentication accelerator are used, it should be set that the holding request withdrawal doesn't demand.

Please set the HRCL register that sets the interrupt level that becomes the standard of the holding request withdrawal demand generation to "10000" in the FR core.

For NMIs, the hold request cancel request occurs regardless of the HRCL register setting. When the encryption/authentication accelerator is used, therefore, NMI input may cause encryption/authentication to fail to result correctly. In that case, the correspondence said that it will execute the encryption/authentication processing under execution again is necessary.

• **Notes as device**

Treatment of Unused Input Pins

It causes the malfunction that the unused input terminal is made open, and do the processing such as 1 stack or 0 stacks.

About Mode pins (MDI2 to MDI0)

Connect these pins with the input buffer by 1 to 1 to prevent the malfunction by the noise, and connect directly to VDD or VSS outside of ASIC.

Operation at start-up

Specify set initialization reset (INIT) with the terminal INITXI when you turn on the power supply.

Moreover, connect "L" level input to the terminal INITXI until the input clock is steady.

About watch dog timer

The watchdog timer function of this macro monitors a program to check whether it delays a reset within a certain period of time. If the program runs out of control and fails to delay the reset, the watchdog timer function resets the CPU.

Therefore, it keeps operating until reset is specified when the watchdog timer function is made effective once.

Exceptionally, the reset postponement is automatically done under the condition that the program execution of CPU stops. Refer to the paragraph of the function explanation of the watchdog timer for the condition of applying to this exception.

There is a possibility that watchdog reset is not generated when entering the above-mentioned state by the reckless driving of the system. In that case, please specify reset (INIT) from external INITX terminal.

Restrictions

• Clock control block
  • Secure the clock stability waiting time at "L" input to INITXI.
  • When entering the standby mode, use the following sequences after using the synchronous standby mode (TBCR:set at the bit8 SYNCS bit of timebase counter control register).

```
(LDI     #value_of_standby, R0)   ; Value_of standby is write data to STCR.
(LDI     #_STCR, R12)             ; _STCR is address (481H) of STCR.
STB      R0, @R12                 ; Write to standby control register (STCR).
LDUB     @R12, R0                 ; STCR read for synchronous standby
LDUB     @R12, R0                 ; Dummy re-read of STCR
NOP
NOP
NOP
NOP
NOP
```

In addition, set the I-flag and the ILM and ICR registers to branch to an interrupt handler when the interrupt handler triggers the microcontroller to return from the standby mode.

  • Please do not do the following when the monitor debugger is used.
  • Please do not set the break point to the above-mentioned instruction row.

CPU

- The instruction fetch is not done from D-bus, and does not set the code area on D-bus RAM.
- Set neither stack area nor the vector table on the instruction RAM.
- The following operations may be performed when the instruction immediately followed by a DIVOU/DIVOS instruction is (a) halted by a user interrupt or NMI, (b) single-stepped, or (c) breaks in response to a data event or emulator menu:
  (1) The D0 and D1 flags are updated in advance.
  (2) An EIT handling routine (user interrupt, NMI, or emulator) is executed.
  (3) Upon returning from the EIT, the DIVOU/DIVOS instruction is executed and the D0 and D1 flags are updated to the same values as in (1) .
- The following operations are performed when the ORCCR/STILM/MOVRi and PS instructions are executed.
  (1) The PS register is updated in advance.
  (2) Executing of EIT processing routine (user interrupt • NMI)
  (3) Upon returning from the EIT, the above instructions are executed and the PS register is updated to the same value as in (1) .
- Since some instructions manipulate the PS register earlier, the following exceptions may cause the interrupt handler to break or the PS flag to update its display setting when the debugger is being used. As the micro-controller is designed to carry out reprocessing correctly upon returning from such an EIT event in either case, it performs operations before and after the EIT as specified.

1. When (a) user interrupt and NMI are accepted or (b) step is executed or (c) break is done by the data event or the menu of the emulator in the instruction immediately before the instruction of DIV0U/DIV0S, the following operation might be done.
   (1) The D0 and D1 flags are updated in advance.
   (2) An EIT handling routine (user interrupt, NMI, or emulator) is executed.
   (1) Upon returning from the EIT, the DIVOU/DIVOS instruction is executed and the D0 and D1 flags are updated to the same values as in (3) .

2. When ORCCR, STILM, MOV Ri, and PS each instruction is executed to permit interrupt with the user interrupt and the NMI factor generated, the following operation is done.
   (1) The PS register is updated in advance.
   (2) The EIT processing routine (user interrupt, NMI or emulator) is executed.
   (3) Upon returning from the EIT, the above instructions are executed and the PS register is updated to the same value as in (1).

- Do not access the data to the cache memory at the control register of the instruction cash and RAM mode immediately before the instruction of RETI.
- If one of the instructions listed below is executed, the SSP or USP* value is not used as the R15 value and, as a result, an incorrect value is written to memory.
- Only ten following kinds of instructions that specify R15 as Ri correspond.

AND	R15, @Rj	ANDH	R15, @Rj	ANDB	R15, @Rj
OR	R15, @Rj	ORH	R15, @Rj	ORB	R15, @Rj
EOR	R15, @Rj	EORH	R15, @Rj	EORB	R15, @Rj
XCHB	@Rj, R15				

* : As for R15, there are no realities. When R15 is accessed from the program, SSP or USP is accessed by the state of "S" flag of the PS register. Please specify general registers other than R15 when ten above-mentioned instructions are described by the assembler.

- External bus interface
  - When the bus width of the area set up as little endian is 32-bit, confine to word (32-bit) access when accessing the relevant area.
  - When enabling prefetch to the area set to the Little endian, give the access to the corresponding area as word (32 bits) access limitation. In the byte and the half word access, it is not possible to access it correctly.

- DMA
  - Do not transfer DMA to instruction RAM.

- Bit Search Module
  - BSD0, BSD1, and the BDSC register are only the word accesses.

■ NOTES OF DEBUG

Step execution of RETI instruction

In an environment where interrupts frequently occur during single-step execution, only the relevant interrupt processing routines are executed repeatedly during single-step execution of the RETI instruction. This will prevent the main routine and low-interrupt-level programs from being executed.

Do not execute step of RETI instruction for escape.

When the relevant interrupt routine no longer requires being debugged, disable the relevant interrupt and perform debugging.

Operand break

Do not set the access which is used for area, including the address of system stack pointer, to the target of data event break.

Interrupt handler to NMI request (tool)

To prevent the malfunction because of the noise problem of DSU pin when ICE is unconnected, the following programs are added to the interrupt handler by the cause flag, which is only set by the break request from ICE. ICE can be used even if this program is added.

Location to added

The following interrupt handler

Interrupt resource : NMI request (tool)
Interrupt number : 13 (decimal), 0D (hexadecimal)
Offset : $3C8_H$
TBR is default address. : $000FFFC8_H$

Additional program

```
STM   (R0, R1)
LDI  #B00H, R0   ; B00H is address of the break resource register.
LDI  #0, R1
STB  R1, @R0     ; Clear the break resource register.
LDM   (R0, R1)
RETI
```

Trace mode

If the trace mode is set to "Full trace mode" during debug (in full trace mode, built-in FIFO is used as output buffer, the trace memory of the main body of ICE is used, and the trace data lost is not occurred), the electric current is increased and D-busDMA access may be lost.

Also, the trace data lost may be occurred.

To take the measures, do not set full trace mode.

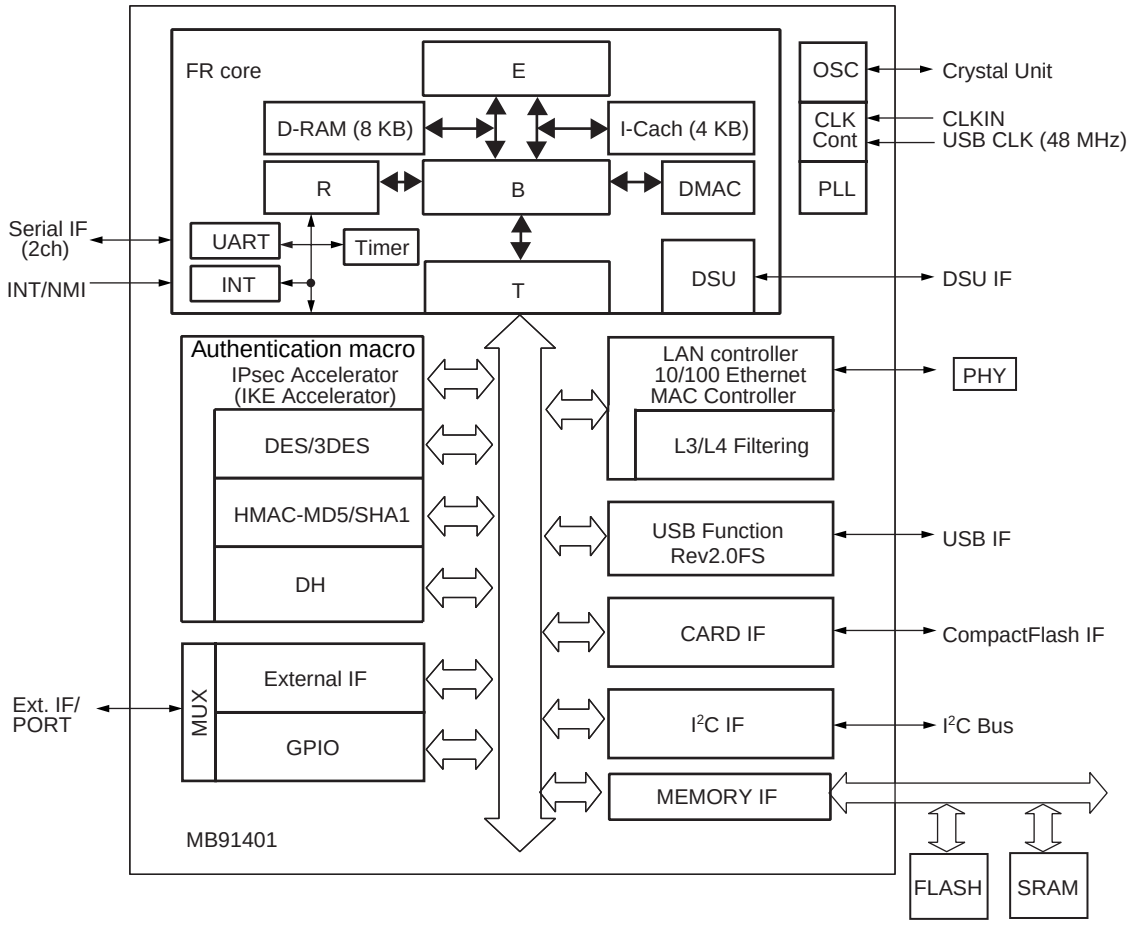
Simultaneous generation of a software break and a user interrupt/NMI

When a software break and a user interrupt/NMI occur simultaneously, the emulator debugger may react as follows.

- The debugger stops pointing to a location other than the programmed breakpoints.
- The halted program is not re-executed correctly.

When these problems are occurred, not only the software break, the hardware break should also be used. Do not set the break to the corresponding location when using monitor debugger.

■ BLOCK DIAGRAM



FR core : CPU, U-Timer, UART, Timer, Interrupt controller, DMAC, Bit search, External interrupt, Memory_IF, Data-RAM, Cache, Bus controller

Peripheral resources : LAN, External_IF, GPIO, Card, Encryption/Authentication, I^2C, USB (Peripheral resource is connected to bus of bus controller.)

■ MEMORY SPACE

• Memory space

The FR family has 4 GByte of logical addresses (2^{32} address) which can be linearly accessed by the CPU.

Direct Addressing Areas

The following address space areas are used as I/O areas.

These areas are called direct addressing areas, in which the address of an operand can be specified directly during an instruction.

The direct addressing area varies as shown below depending on the size of access data:

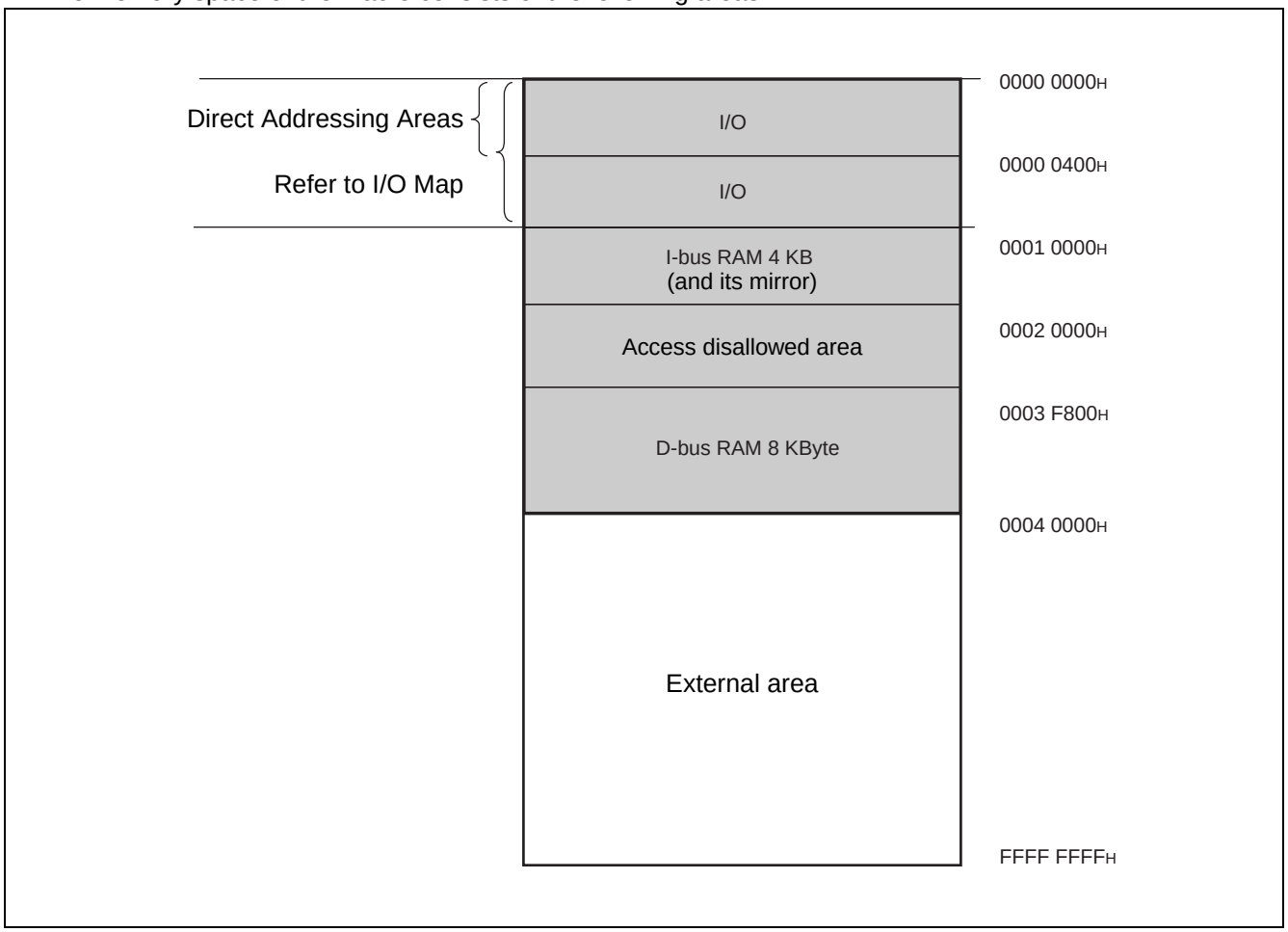
→ byte data access : 0-0FF$_H$

→ half word data access : 0-1FF$_H$

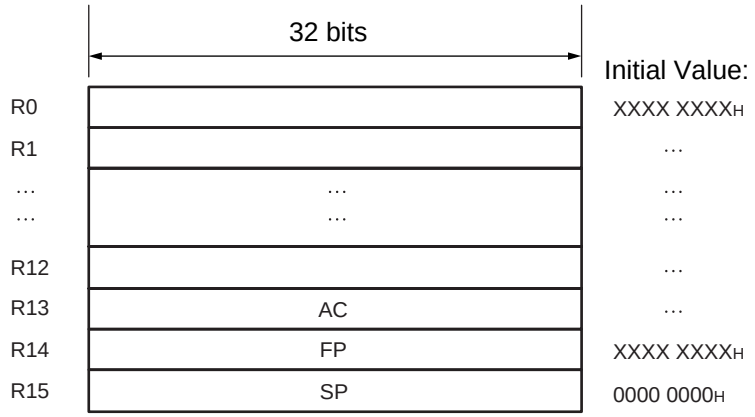
→ word data access : 0-3FF$_H$

• Memory Map

The memory space of the macro consists of the following areas.



■ GENERAL PURPOSE REGISTERS



Registers R0 to R15 are general-purpose registers. The registers are used as the accumulator and memory access pointers for CPU operations.

Of these 16 registers, the registers listed below are intended for special applications, for which some instructions are enhanced.

R13: Virtual accumulator

R14: frame pointer

R15:Stack pointer

The initial values of R0 to R14 after a reset are indeterminate. R15 is initialized to 00000000_H (SSP value).

■ MODE SETTINGS

The FR family uses the mode pins (MDI2 to MDI0) and the mode register (MODR) to set the operation mode.

• Mode Pins

Three mode pins MDI[2], MDI[1], and MDI[0] are used to specify a mode vector fetch or test mode.

Mode pins MDI2 to MDI0	Mode name	Reset vector access area	Remarks
0 0 0	Reserved	—	
0 0 1	external ROM mode vector	External	Bus width is set by the mode data.
0 1 0	User circuit test	—	FR stops (with clock signal supplied).
0 1 1	Reserved	—	
1 0 0	Reserved	—	
1 0 1	Reserved	—	
1 1 0	Reserved	—	
1 1 1	Reserved	—	

Setting MDI2 to MDI0 to "010", USRTEST is set to "1" and the device operates in the user circuit test mode. The FR71 core is suspended in the user circuit test mode while SYSCLK and MCLKO are operating. The reserved modes include the FR71 core test mode. In this case, the signal at the FRTEST pin becomes "1" and enters the FR71 core test mode. If the FRTEST pin = "1", that circuit configuration is required which allows the separately defined pins of the FR71 core to be controlled and monitored from the outside of the chip.

• Mode Register (MODR)

The data written to the mode register (MODR) by hardware using a mode vector fetch is called mode data.

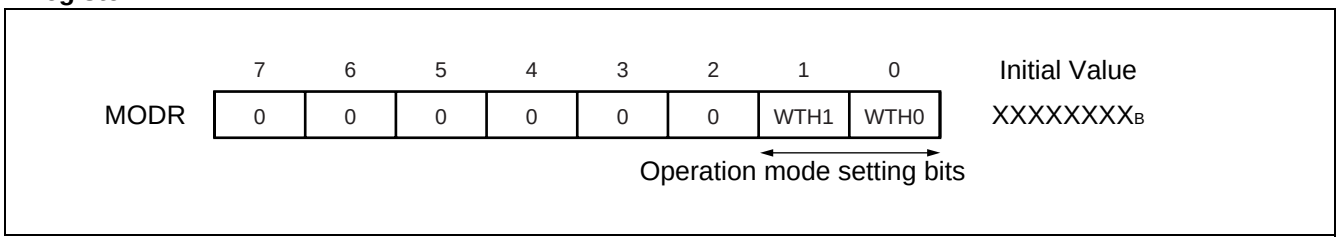
When this register is set by hardware, the CPU operates in the operation mode corresponding to the register setting.

The mode register is set only by an INIT-level reset cause. The user program cannot access this register.

However, as an exception, when the macro shifts to emulation mode by INTE instruction, or shifts to emulation mode by a break at a debug using ICE, this register is mapped at 0000_07FD$_H$. Select this function when using ICE, perform the mode data setting before the program loading by writing a appropriate value to this register.

Note : No data is existed in the address (0000_07FF$_H$) in the mode register of the FR family.

• Register



[bit7 to bit2] Reserved bit

Be sure to set this bit to “000000”. Setting them to any other value may result in an unpredictable operation.

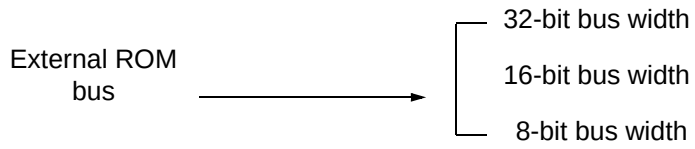
[bit1, bit0] WTH1, WTH0 (Bus width setting bits)

These bits specify the bus width. The value of the bits is set in the DBW1 and DBW0 bits in ACR0 (CSO area). Set these bits to a value other than “11”.

WTH1	WTH0	Function	Remarks
0	0	8-bit bus width	External bus mode
0	1	16-bit bus width	External bus mode
1	0	32-bit bus width	External bus mode
1	1	Setting disabled	

- **Operation mode**

In the operation mode, there are a bus mode and an access mode.



Bus mode

In bus mode, the operations of internal ROM and the external access functions are controlled according to the mode setting pins (MD2 to MD0) and the values of mode data.

Although the FR71 architecture supports this bus mode, this macro cannot use the single-chip or internal ROM/external bus mode but can use the external ROM/external bus mode only.

Access mode

Access mode indicates the mode that controls the external data bus width, and is specified by the WTH1/WTH0 bits, and the DBW1/DBW0 bits within ACR0 to ACR7 (Area Configuration Registers).

Bus mode

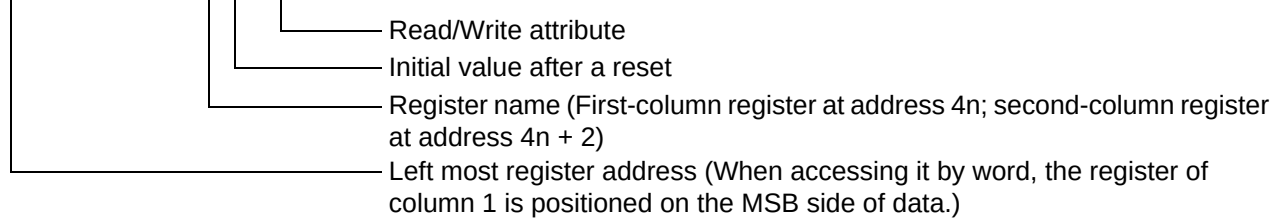
The FR family has three bus modes described below. Please refer to “■ MEMORY SPACE” for details.

■ I/O MAP

This shows the location of the various peripheral resource registers in the memory space.

[How to read the table]

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000_0000H | 0000_003CH	—				Reserved
0000_0040H	EIRR [R/W] 00000000	ENIR [R/W] 00000000	ELVR [R/W] 00000000 00000000		Ext Int



Note : Initial values of register bits are represented as follows :

"1" : Initial Value "1"
"0" : Initial Value "0"
"X" : Initial Value "X"
"-" : Access prohibited in reserved area.

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000_0000H to 0000_003CH	—				Reserved
0000_0040H	EIRR [R/W] 00000000	ENIR [R/W] 00000000	ELVR [R/W] 00000000 00000000		Ext Int
0000_0044H	DICR [R/W] -------0	HRCL [R/W] 0-11111	—		DLYI/I-unit
0000_0048H	TMRLR0 [W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0
0000_004CH	—		TMCSR0 [R/W] ----0000 00000000		
0000_0050H	TMRLR1 [W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX		Reload Timer 1
0000_0054H	—		TMCSR1 [R/W] ----0000 00000000		
0000_0058H	TMRLR2 [W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX		Reload Timer 2
0000_005CH	—		TMCSR2 [R/W] ----0000 00000000		

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000_0060H	SSR0 [R/W] 00001-00	SIDR0 [R/W] XXXXXXXX	SCR0 [R/W] 00000100	SMR0 [R/W] 00--0-0-	UART0
0000_0064H	UTIM0 [R] (UTIMR0 [W]) 00000000 00000000		DRCL0 [W] --------	UTIMC0 [R/W] 0--00001	U-TIMER0
0000_0068H	SSR1 [R/W] 00001-00	SIDR1 [R/W] XXXXXXXX	SCR1 [R/W] 00000100	SMR1 [R/W] 00--0-0-	UART1
0000_0048H	UTIM1 [R] (UTIMR1 [W]) 00000000 00000000		DRCL1 [W] --------	UTIMC1 [R/W] 0--00001	U-TIMER1
0000_0070H to 0000_01FCH	—				Reserved
0000_0200H	DMACA0 [R/W] 00000000 00000000 0000XXXX XXXXXXXX				DMAC
0000_0204H	DMACB0 [R/W] 00000000 00000000 00000000 00000000				
0000_0208H	DMACA1 [R/W] 00000000 00000000 0000XXXX XXXXXXXX				
0000_020CH	DMACB1 [R/W] 00000000 00000000 00000000 00000000				
0000_0210H	DMACA2 [R/W] 00000000 00000000 0000XXXX XXXXXXXX				
0000_0214H	DMACB2 [R/W] 00000000 00000000 00000000 00000000				
0000_0218H	DMACA3 [R/W] 00000000 00000000 0000XXXX XXXXXXXX				
0000_021CH	DMACB3 [R/W] 00000000 00000000 00000000 00000000				
0000_0220H	DMACA4 [R/W] 00000000 00000000 0000XXXX XXXXXXXX				
0000_0224H	DMACB4 [R/W] 00000000 00000000 00000000 00000000				
0000_0228H to 0000_023CH	—				Reserved
0000_0240H	DMACR [R/W] 0XX00000 XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
0000_0244H to 0000_0300H	—				Reserved
0000_0304H	—			ISIZE [R/W] ------10	Instruction Cache

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000_0308H to 0000_03E0H	—				Reserved
0000_03E4H	—			ICHRC [R/W] 0-000000	Instruction Cache
0000_03E8H to 0000_03ECH	—				Reserved
0000_03F0H	BSD0 [W] XXXXXXXX XXXXXXXX		XXXXXXXX XXXXXXXX		Bit Search Module
0000_03F4H	BSD1 [R/W] XXXXXXXX XXXXXXXX		XXXXXXXX XXXXXXXX		
0000_03F8H	BSDC [W] XXXXXXXX XXXXXXXX		XXXXXXXX XXXXXXXX		
0000_03FCH	BSRR [R] XXXXXXXX XXXXXXXX		XXXXXXXX XXXXXXXX		
0000_0400H to 0000_043CH	—				Reserved
0000_0440H	ICR00[R/W] ---11111	ICR01[R/W] ---11111	ICR02[R/W] ---11111	ICR03[R/W] ---11111	Interrupt Control Unit
0000_0444H	ICR04[R/W] ---11111	ICR05[R/W] ---11111	ICR06[R/W] ---11111	ICR07[R/W] ---11111	
0000_0448H	ICR08[R/W] ---11111	ICR09[R/W] ---11111	ICR10[R/W] ---11111	ICR11[R/W] ---11111	
0000_044CH	ICR12[R/W] ---11111	ICR13[R/W] ---11111	ICR14[R/W] ---11111	ICR15[R/W] ---11111	
0000_0450H	ICR16[R/W] ---11111	ICR17[R/W] ---11111	ICR18[R/W] ---11111	ICR19[R/W] ---11111	
0000_0454H	ICR20[R/W] ---11111	ICR21[R/W] ---11111	ICR22[R/W] ---11111	ICR23[R/W] ---11111	
0000_0458H	ICR24[R/W] ---11111	ICR25[R/W] ---11111	ICR26[R/W] ---11111	ICR27[R/W] ---11111	
0000_045CH	ICR28[R/W] ---11111	ICR29[R/W] ---11111	ICR30[R/W] ---11111	ICR31[R/W] ---11111	
0000_0460H	ICR32[R/W] ---11111	ICR33[R/W] ---11111	ICR34[R/W] ---11111	ICR35[R/W] ---11111	
0000_0464H	ICR36[R/W] ---11111	ICR37[R/W] ---11111	ICR38[R/W] ---11111	ICR39[R/W] ---11111	
0000_0468H	ICR40[R/W] ---11111	ICR41[R/W] ---11111	ICR42[R/W] ---11111	ICR43[R/W] ---11111	

(Continued)

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000_046C$_H$	ICR44[R/W] ---11111	ICR45[R/W] ---11111	ICR46[R/W] ---11111	ICR47[R/W] ---11111	Interrupt Control Unit
0000_0470$_H$ to 0000_047C$_H$	—	—	—	—	Reserved
0000_0480$_H$	RSRR [R/W] 10000000*2	STCR [R/W] 00110011*2	TBCR [R/W] 00XXXX00*1	CTBR [R/W] XXXXXXXX	Clock Control Unit
0000_0484$_H$	— Access disallowed	WPR [W] XXXXXXXX	DIVR0 [R/W] 00000011*1	DIVR1 [R/W] 00000000	
0000_0488$_H$ to 0000_063F$_H$	—				Reserved
0000_0640$_H$	ASR0 [R/W] 00000000 00000000		ACR0 [R/W] 1111**00 00000000*3		Memory IF
0000_0644$_H$	ASR1 [R/W] XXXXXXXX XXXXXXXX		ACR1 [R/W] XXXXXXXX XXXXXXXX		
0000_0648$_H$	ASR2 [R/W] XXXXXXXX XXXXXXXX		ACR2 [R/W] XXXXXXXX XXXXXXXX		
0000_064C$_H$	ASR3 [R/W] XXXXXXXX XXXXXXXX		ACR3 [R/W] XXXXXXXX XXXXXXXX		
0000_0650$_H$	ASR4 [R/W] XXXXXXXX XXXXXXXX		ACR4 [R/W] XXXXXXXX XXXXXXXX		
0000_0654$_H$	ASR5 [R/W] XXXXXXXX XXXXXXXX		ACR5 [R/W] XXXXXXXX XXXXXXXX		
0000_0658$_H$	ASR6 [R/W] XXXXXXXX XXXXXXXX		ACR6 [R/W] XXXXXXXX XXXXXXXX		
0000_065C$_H$	ASR7 [R/W] XXXXXXXX XXXXXXXX		ACR7 [R/W] XXXXXXXX XXXXXXXX		
0000_0660$_H$	AWR0 [R/W] 01111111 11111111		AWR1 [R/W] XXXXXXXX XXXXXXXX		
0000_0664$_H$	AWR2 [R/W] XXXXXXXX XXXXXXXX		AWR3 [R/W] XXXXXXXX XXXXXXXX		
0000_0668$_H$	AWR4 [R/W] XXXXXXXX XXXXXXXX		AWR5 [R/W] XXXXXXXX XXXXXXXX		
0000_066C$_H$	AWR6 [R/W] XXXXXXXX XXXXXXXX		AWR7 [R/W] XXXXXXXX XXXXXXXX		
0000_0670$_H$	MCRA XXXXXXXX	MCRB XXXXXXXX	—		
0000_0674$_H$	—				
0000_0678$_H$	IOWR0 [R/W] XXXXXXXX	IOWR1 [R/W] XXXXXXXX	IOWR2 [R/W] XXXXXXXX	—	

(Continued)

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000_067C$_H$	—				Memory IF
0000_0680$_H$	CSER [R/W] 00000001	CHER [R/W] XXXXXXX1	—	TCR [R/W] 00000000*1	
0000_0684$_H$	RCR 00XXXXXX 00XXXXXX		—		
0000_0688$_H$ to 0000_0FFC$_H$	—				Reserved

*1 : An initial value is a different register at the reset level. The display is the one at the INIT level.

*2 : An initial value is a different register at the reset level. The display is due to the INIT level by INITX.

*3 : An initial value is set by the WTH bit of the mode vector.

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000_1000$_H$	DMASA0 [R/W] XXXXXXXX XXXXXXXX		XXXXXXXX XXXXXXXX		DMAC
0000_1004$_H$	DMADA0 [R/W] XXXXXXXX XXXXXXXX		XXXXXXXX XXXXXXXX		
0000_1008$_H$	DMASA1 [R/W] XXXXXXXX XXXXXXXX		XXXXXXXX XXXXXXXX		
0000_100C$_H$	DMADA1 [R/W] XXXXXXXX XXXXXXXX		XXXXXXXX XXXXXXXX		
0000_1010$_H$	DMASA2 [R/W] XXXXXXXX XXXXXXXX		XXXXXXXX XXXXXXXX		
0000_1014$_H$	DMADA2 [R/W] XXXXXXXX XXXXXXXX		XXXXXXXX XXXXXXXX		
0000_1018$_H$	DMASA3 [R/W] XXXXXXXX XXXXXXXX		XXXXXXXX XXXXXXXX		
0000_101C$_H$	DMADA3 [R/W] XXXXXXXX XXXXXXXX		XXXXXXXX XXXXXXXX		
0000_1020$_H$	DMASA4 [R/W] XXXXXXXX XXXXXXXX		XXXXXXXX XXXXXXXX		
0000_1024$_H$	DMADA4 [R/W] XXXXXXXX XXXXXXXX		XXXXXXXX XXXXXXXX		
0000_1028$_H$ to 0000_FFFC$_H$	—				Reserved

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
010F_0000H	BSR[R] 00000000	BCR[R/W] 00000000	CCR[R/W] 10000000	ADR[R/W] 1XXXXXXX	I²C
010F_0004H	DAR[R/W] XXXXXXXX	— —	— —	BC2R[R/W] 00XX0000	
010F_0008H to 010F_FFFFH	(Reserved) —				

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0110_0000H	DLCR0* 0X000000	DLCR1[R, W] 00000000	DLCR2* 00000000	DLCR3[R/W] 00000000	LAN controller
0110_0004H	DLCR4* 00000010	DLCR5* 01000001	DLCR6* 10000000	DLCR7* 00000000	
0110_0008H	DLCR8[R/W] 00000000	DLCR9[R/W] 00000000	DLCR10[R/W] 00000000	DLCR11[R/W] 00000000	Bank 0
0110_000CH	DLCR12[R/W] 00000000	DLCR13[R/W] 00000000	— —	— —	
0110_0008H	MAR8[R/W] 00000000	MAR9[R/W] 00000000	MAR10[R/W] 00000000	MAR11[R/W] 00000000	Bank 1
0110_000CH	MAR12[R/W] 00000000	MAR13[R/W] 00000000	MAR14[R/W] 00000000	MAR15[R/W] 00000000	
0110_0008H	— —	— —	BMPR10* 00000000	BMPR11* 00000111	Bank 2
0110_000CH	BMPR12* 00000000	— —	BMPR14* 00000000	— —	
0110_0010H	BMPR8 00000000-00000000		[R/W] 00000000-00000000		
0110_0014H	FILTER_CMD [R/W] XXXXXXXX	— —	— —		
0110_0018H	FILTER_STATUS [R] XXXXXXXX	— —	— —		
0110_001CH	FILTER_DATA [R/W] XXXXXXXX	— —	— —		
0110_0020H	FL_CONTROL [R/W] XXXXXXXX	— —	— —		
0110_0024H	FL_SUBNET [R/W] XXXXXXXX	— —	— —		

(Continued)

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0110_0028H	SMI_CMD[R/W] 00000000-00000000		— —		SIM IF
0110_002CH	SMI_CMD_ST [R/W] 00XXXXXX	— —	— —		
0110_0030H	SMI_DATA [R/W] 00000000-00000000		— —		
0110_0034H	SMI_POLLINTVL [R/W] 00000000-00000000		— —		
0110_0038H	SMI_PHY_ADD [R/W] 00000XXX	— —	— —		SIM IF
0110_003CH	SMI_CONTROL [R/W] 111XXXXX	— —	— —		
0110_0040H	SMI_STATUS[R] XXXXXXXX	— —	— —		
0110_0044H	SMI_INTENABLE [R/W] 0XXXXXXX	— —	— —		
0110_0048H	SMI_MDCDIV [R/W] 01011XXX	— —	— —		

* : The attribute is different according to the bit.

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0114_0000H	EXIFRXDR [R] 00000000-00000000		00000000-00000000		External IF
0114_0004H	EXIFTXDR [W] 00000000-00000000		00000000-00000000		
0114_0008H	EXIFRXR[R] 00000000-00000000		— —		
0114_000CH	EXIFTXR[W] 00000000-00000000		— —		
0114_0010H	EXIFCR[W] 00000000-0XXXXXXX		— —		
0114_0014H	EXIFSR[R] 00000000-00XXXXXX		— —		
0114_0018H	EXIFRXSR [R] 00000000-00000000		00000000-00000000		
0114_001CH	EXIFTXSR [R] 00000000-00000000		00000000-00000000		
0114_0020H	—		PIOCR[R/W] 00000000		GPIO
0114_0024H	—	—	PIODR[R/W] Connecting destination		

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0500_03E0H	IR[R/W] 00000000	DR[R/W] 10000011	(Reserved) —	RR[R/W] 00000000	Compact FLASH IF
0501_0000H to 0501_07FFH	AMR (Attribute Memory Area : window 0)				
0501_1000H to 0501_17FFH	CMR (Common Memory Area : window 1)				

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0540_0000H	FIFO0out[R] XXXXXXXX-XXXXXXXX		FIFO0in[W] XXXXXXXX-XXXXXXXX		USB
0540_0004H	FIFO1[R] XXXXXXXX-XXXXXXXX		FIFO2[W] XXXXXXXX-XXXXXXXX		
0540_0008H	FIFO3[W] XXXXXXXX-XXXXXXXX		— —		
0540_000CH to 0540_001FH	(Reserved) —				
0540_0020H	— —		CONT1[R/W] XXXXX0XX-XXX00000		
0540_0024H	CONT2[R/W] XXXXXXXX_XXX00000		CONT3[R/W] XXXXXXXX_XXX00000		
0540_0028H	CONT4[R/W] XXXXXXXX_XXX00000		CONT5[R/W] XXXXXXXX_XXXX00XX		
0540_002CH	CONT6[R/W] XXXXXXXX_XXXX00XX		CONT7[R/W] XXXXXXXX_XXX00000		
0540_0030H	CONT8[R/W] XXXXXXXX_XXX00000		CONT9[R/W] XXXXXXXX_0XXX0000		
0540_0034H	CONT10[R/W] XXXX0000_X000000X		TTSIZE[R/W] 00010001-00010001		
0540_0038H	TRSIZE[R/W] 00010001-00010001		— —		
0540_003CH to 0540_003FH	(Reserved) —				
0540_0040H	RSIZE0[R] XXXXXXXX-XXXX0000		— —		
0540_0044H	RSIZE1[R] XXXXXXXX-X0000000		— —		
0540_0048H to 0540_005FH	(Reserved) —				USB
0540_0060H	— —		ST1[R/W] XXXXXX00-00000000		
0540_0064H	— —		— —		

(Continued)

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0540_0068H	ST2[R] XXXXXXXX-X0000000		ST3[R/W] XXXXXXXX-XXX00000		USB
0540_006CH	ST4[R] XXXXX000-00000000		ST5[R/W] XXXX0XXX-XX000000		
0540_0070H to 0540_007BH	(Reserved) —				
0540_007CH	—		RESET[R/W] XXXXXXXX-XXXXXX00		
0540_0080H to 0540_FFFFH	(Reserved) —				

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0580_0000H	MACRORR[W/R] 00000000-00000001		CARDSR[R/W] 00000000-00000000		Chip Register
0580_0004H	CARDIMR[R/W] 00000000-00000000		CARDISR[R] 00000000-00000000		
0580_0008H	USBPLLRP[R/W] 00000000-00000000		— —		

■ INTERRUPT VECTOR

Interrupt source	Interrupt number		Interrupt level	Offset	Address of TBR default	RN
	Decimal	Hexa-decimal				
Reset	0	00	—	3FC$_H$	000FFFFC$_H$	—
Mode vector	1	01	—	3F8$_H$	000FFFF8$_H$	—
System reserved	2	02	—	3F4$_H$	000FFFF4$_H$	—
System reserved	3	03	—	3F0$_H$	000FFFF0$_H$	—
System reserved	4	04	—	3EC$_H$	000FFFEC$_H$	—
System reserved	5	05	—	3E8$_H$	000FFFE8$_H$	—
System reserved	6	06	—	3E4$_H$	000FFFE4$_H$	—
Coprocessor absent trap	7	07	—	3E0$_H$	000FFFE0$_H$	—
Coprocessor error trap	8	08	—	3DC$_H$	000FFFDC$_H$	—
INTE instruction	9	09	—	3D8$_H$	000FFFD8$_H$	—
Instruction break exception	10	0A	—	3D4$_H$	000FFFD4$_H$	—
Operand break trap	11	0B	—	3D0$_H$	000FFFD0$_H$	—
Step trace trap	12	0C	—	3CC$_H$	000FFFCC$_H$	—
NMI request (tool)	13	0D	—	3C8$_H$	000FFFC8$_H$	—
Undefined instruction exception	14	0E	—	3C4$_H$	000FFFC4$_H$	—
NMI request	15	0F	F$_H$ fixed	3C0$_H$	000FFFC0$_H$	—
Ethernet MAC IF	16	10	ICR00	3BC$_H$	000FFFBC$_H$	4
Authentication macro	17	11	ICR01	3B8$_H$	000FFFB8$_H$	5
IPSec Accelerator/Code macro	18	12	ICR02	3B4$_H$	000FFFB4$_H$	8
EX IF/GPIO	19	13	ICR03	3B0$_H$	000FFFB0$_H$	9
USB/I^{2}C/CARD IF	20	14	ICR04	3AC$_H$	000FFFAC$_H$	—
External interrupt 5	21	15	ICR05	3A8$_H$	000FFFA8$_H$	—
External interrupt 6	22	16	ICR06	3A4$_H$	000FFFA4$_H$	—
External interrupt 7	23	17	ICR07	3A0$_H$	000FFFA0$_H$	—
Reload timer 0	24	18	ICR08	39C$_H$	000FFF9C$_H$	6
Reload timer 1	25	19	ICR09	398$_H$	000FFF98$_H$	7
Reload timer 2	26	1A	ICR10	394$_H$	000FFF94$_H$	—
UART0 (Reception completed)	27	1B	ICR11	390$_H$	000FFF90$_H$	0
UART1 (Reception completed)	28	1C	ICR12	38C$_H$	000FFF8C$_H$	1
UART0 (RX completed)	29	1D	ICR13	388$_H$	000FFF88$_H$	2
UART1 (RX completed)	30	1E	ICR14	384$_H$	000FFF84$_H$	3
DMAC0 (end error) Ethernet MAC IF	31	1F	ICR15	380$_H$	000FFF80$_H$	—
DMAC1 (end error) External IF	32	20	ICR16	37C$_H$	000FFF7C$_H$	—
DMAC2 (end error) USB	33	21	ICR17	378$_H$	000FFF78$_H$	—

(Continued)

Interrupt source	Interrupt number		Interrupt level	Offset	Address of TBR default	RN
	Decimal	Hexa-decimal				
DMAC3 (end, error)	34	22	ICR18	374H	000FFF74H	—
DMAC4 (end, error)	35	23	ICR19	370H	000FFF70H	—
System reserved	36	24	ICR20	36CH	000FFF6CH	—
System reserved	37	25	ICR21	368H	000FFF68H	—
System reserved	38	26	ICR22	364H	000FFF64H	—
System reserved	39	27	ICR23	360H	000FFF60H	—
System reserved	40	28	ICR24	35CH	000FFF5CH	—
System reserved	41	29	ICR25	358H	000FFF58H	—
System reserved	42	2A	ICR26	354H	000FFF54H	—
System reserved	43	2B	ICR27	350H	000FFF50H	—
System reserved	44	2C	ICR28	34CH	000FFF4CH	—
U-TIMER0	45	2D	ICR29	348H	000FFF48H	—
U-TIMER1	46	2E	ICR30	344H	000FFF44H	—
Timebase timer overflow	47	2F	ICR31	340H	000FFF40H	—
System reserved	48	30	ICR32	33CH	000FFF3CH	—
System reserved	49	31	ICR33	338H	000FFF38H	—
System reserved	50	32	ICR34	334H	000FFF34H	—
System reserved	51	33	ICR35	330H	000FFF30H	—
System reserved	52	34	ICR36	32CH	000FFF2CH	—
System reserved	53	35	ICR37	328H	000FFF28H	—
System reserved	54	36	ICR38	324H	000FFF24H	—
System reserved	55	37	ICR39	320H	000FFF20H	—
System reserved	56	38	ICR40	31CH	000FFF1CH	—
System reserved	57	39	ICR41	318H	000FFF18H	—
System reserved	58	3A	ICR42	314H	000FFF14H	—
System reserved	59	3B	ICR43	310H	000FFF10H	—
System reserved	60	3C	ICR44	30CH	000FFF0CH	—
System reserved	61	3D	ICR45	308H	000FFF08H	—
System reserved	62	3E	ICR46	304H	000FFF04H	—
Delay interrupt source bit	63	3F	ICR47	300H	000FFF00H	—
System reserved (Used by REALOS*)	64	40	—	2FCH	000FFEFCH	—
System reserved (Used by REALOS*)	65	41	—	2F8H	000FFEF8H	—
System reserved	66	42	—	2F4H	000FFEF4H	—
System reserved	67	43	—	2F0H	000FFEF0H	—

(Continued)

(Continued)

Interrupt source	Interrupt number		Interrupt level	Offset	Address of TBR default	RN
	Decimal	Hexa-decimal				
System reserved	68	44	—	2EC$_H$	000FFEEC$_H$	—
System reserved	69	45	—	2E8$_H$	000FFEE8$_H$	—
System reserved	70	46	—	2E4$_H$	000FFEE4$_H$	—
System reserved	71	47	—	2E0$_H$	000FFEE0$_H$	—
System reserved	72	48	—	2DC$_H$	000FFEDC$_H$	—
System reserved	73	49	—	2D8$_H$	000FFED8$_H$	—
System reserved	74	4A	—	2D4$_H$	000FFED4$_H$	—
System reserved	75	4B	—	2D0$_H$	000FFED0$_H$	—
System reserved	76	4C	—	2CC$_H$	000FFECC$_H$	—
System reserved	77	4D	—	2C8$_H$	000FFEC8$_H$	—
System reserved	78	4E	—	2C4$_H$	000FFEC4$_H$	—
System reserved	79	4F	—	2C0$_H$	000FFEC0$_H$	—
Used by INT instruction	80 to 255	50 to FF	—	2BC$_H$ to 000$_H$	000FFEBC$_H$ to 000FFC00$_H$	—

(2) NMI (Non Maskable Interrupt)

NMIs have the highest priority among the interrupt sources handled by this module.
An NMI is always selected whenever other types of interrupt sources occur at the same time.

- If an NMI occurs, the interrupt controller passes the information to the CPU :
  Interrupt level : 15 (01111$_B$)
  Interrupt number : 15 (0001111$_B$)
- NMI detection
  NMIs are set and detected by the external interrupt/NMI controller. This module only generates an interrupt level, interrupt number, and MHALTI upon NMI request.
- Suppressing DMA transfer upon NMI request
  When an NMI request occurs, the MHALTI bit in the HRCL register is set to "1", suppressing DMA transfer. To permit DMA transfer, clear the MHALTI bit to "0" at the end of the NMI routine.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter		Symbol	Rating		Unit	Remarks
			Min	Max		
Power supply voltage*1	I/O	V_{DDE}	VSS − 0.3	VSS + 4.0	V	
	Internal	V_{DDI}	VSS − 0.3	VSS + 2.5	V	
Analog power supply voltage		PLLVDD	VSS − 0.3	VSS + 4.0	V	*2
Input voltage*1		V_I	VSS − 0.3	VDDE + 0.3	V	
Output voltage*1		V_O	VSS − 0.3	VDDE + 0.3	V	
“L” level maximum output current		I_{OL}	—	T.B.D	mA	*3
“L” level average output current		I_{OLAV}	—	T.B.D	mA	*4
“L” level total maximum output current		ΣI_{OL}	—	T.B.D	mA	
“L” level total average output cur rent		ΣI_{OLAV}	—	T.B.D	mA	*5
“H” level maximum output current		I_{OH}	—	T.B.D	mA	*3
“H” level average output current		I_{OHAV}	—	T.B.D	mA	*4
“H” level total maximum output current		ΣI_{OH}	—	T.B.D	mA	
“H” level total average output cur rent		ΣI_{OHAV}	—	T.B.D	mA	*5
Power consumption		P_D	—	T.B.D	mW	
Operating temperature		Ta	− 10	70	°C	
Storage temperature		Tstg	− 55	150	°C	

*1 : This parameter is based on VSS = PLLVSS = 0 V.

*2 : Note that analog power supply voltage and input voltage do not exceed VDDE + 0.3 V at power on.

*3 : The maximum output current is the peak value for a single pin.

*4 : The average output current is the average current for a single pin over a period of 100 ms.

*5 : The total average output current is the average current for all pins over a period of 100 ms.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Notes :
- Apply equal potential to all of the VDDE pins.
- Apply equal potential to all of the VDDI pins.
- Fix all of the VSS pins at 0 V.
- Leave N.C. pins open.

2. Recommended Operating Conditions

(VSS = PLLVSS = 0 V)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Power supply voltage	I/O	V_{DDE}	3.0	3.3	3.6	V
	Internal	V_{DDI}	1.65	1.8	1.95	V
Analog power supply voltage		PLLVDD	VSS + 3.0	—	VDDE	V
Operating temperature		Ta	− 10	—	70.0	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

- Other than USB

(VSS = PLLVSS = 0 V)

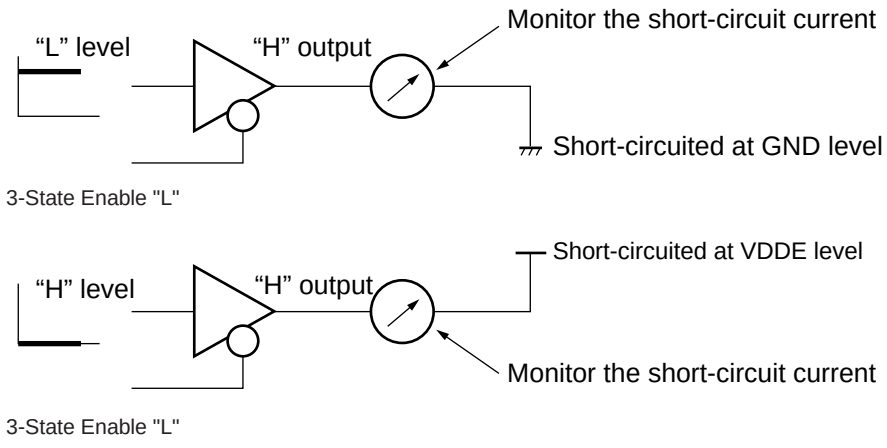
Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
"H" level input voltage	V_{IH}	—	—	2.0	—	VDDE + 0.3	V
"L" level input voltage	V_{IL}	—	—	VSS – 0.3	—	0.8	V
"H" level output voltage	V_{OH}	—	V_{DDE} = 3.0 V, I_{OH} = 4.0 mA	VDDE – 0.5	—	—	V
"L" level output voltage	V_{OL}	—	V_{DDE} = 3.0 V, I_{OH} = 4.0 mA	—	—	0.4	V
Input leak current	I_{LI}	—	V_{DDE} = 3.6 V, $V_{SS} < V_I < V_{DDE}$	—	—	± 5	µA
Pull-up resistance	R_{PULU}	TCK/TRST/TMS/ TDI/TDO/ CFCD2X/ CFCD1X/ CFVS1X/CFRDY/ CFWAITX	—	10	33	80	kΩ
Pull-down resistance	R_{PULD}	CFRESET	—	10	33	80	kΩ
Power supply current	I_{CC}	VDDE	V_{DDI} = 1.8 V, V_{DDE} = 3.3 V, fc = 50 MHz	—	—	T.B.D	mA
		VDDI		—	—	T.B.D	mA
Input capacitance	C_{IN}	Without power supply	—	—	18	—	pF

• USB

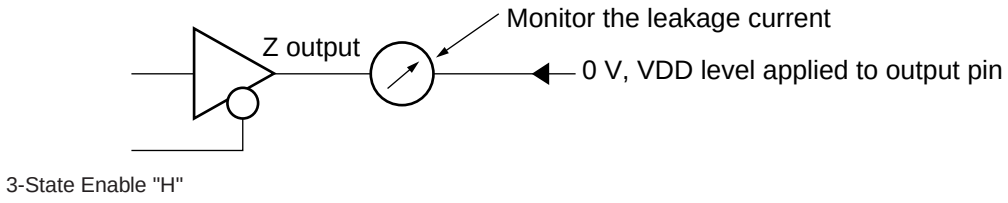
(VSS = PLLVSS = 0 V)

Parameter	Symbol	Pin	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH}	—	I_{OH} = – 100 µA	VDDE – 0.2	—	VDDE	V	
"L" level output voltage	V_{OL}	—	I_{OL} = 100 µA	0	—	0.2	V	
"H" level output current	I_{OH}	—	$V_{OH} = V_{DDE} – 0.4$ V	– 20	—	—	mA	
"L" level output current	I_{OL}	—	V_{OL} = 0.4 V	20	—	—	mA	
output short circuit current	I_{OS}	—	—	—	—	300	mA	*1
Input leak current	I_{LZ}	—	—	—	—	± 5	µA	*2

*1 : <About the output short-circuit current>
Output short-circuit current I_{OS} is the maximum current that flows when the output pin is connected to V_{DDE} or V_{SS} (within the maximum rating) . The current is "the short-circuit current per differential output pin." As the USB I/O buffer is a differential output, the short-circuit current should be considered for both of the output pins.



*2 : <About Measurement of Z leakage current I_{LZ}>
Input leakage current I_{LZ} is measured with the USB I/O buffer in the high-impedance state when the V_{DDE} or V_{SS} voltage is applied to the bidirectional pin.



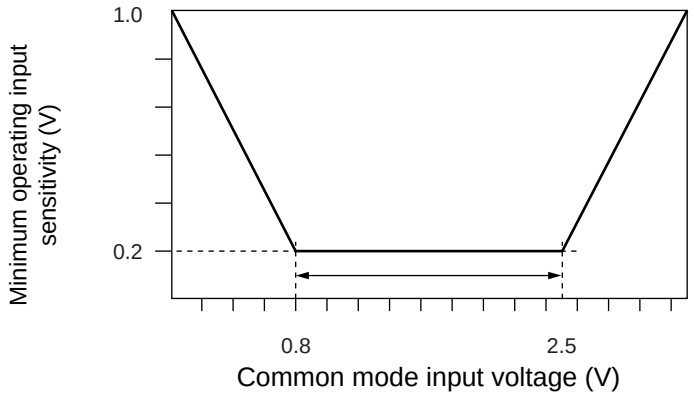
USB Specification Revision 1.1

Parameter		Symbol	Value		Unit	Remarks
			Min	Max		
Input Levels						
	High (driven)	V_{IH}	2.0	—	V	*1
	Low	V_{IL}	—	0.8	V	*1
	Diffential Input Sensitivity	V_{DI}	0.2	—	V	*2
	Differential Common Mode Range	V_{CM}	0.8	2.5	V	*2
Output Levels						
	High (driven)	V_{OH}	0.0	0.3	V	*3
	Low	V_{OL}	2.8	3.6	V	*3
	Output Signal Crossover Voltage	V_{CRS}	1.3	2.0	V	*4
Terminations						
	Bus Pull-up Resistor on Upstream Port	R_{PU}	1.425	1.575	kΩ	1.5 kΩ ± 5%
	Termination Voltage for Upstream Port Pull-up	V_{TERM}	3.0	3.6	V	*5

*1 : <Input Levels V_{IH}, V_{IL}>
The switching threshold voltage of the USB I/O buffer's single-end receiver is set within the range from $V_{IL\ (Max)}$ = 0.8 V to $V_{IH\ (Min)}$ = 2.0 V (TTL input standard) .
For V_{IH} and V_{IL}, the LSI has some hysteresis to reduce noise susceptibility.

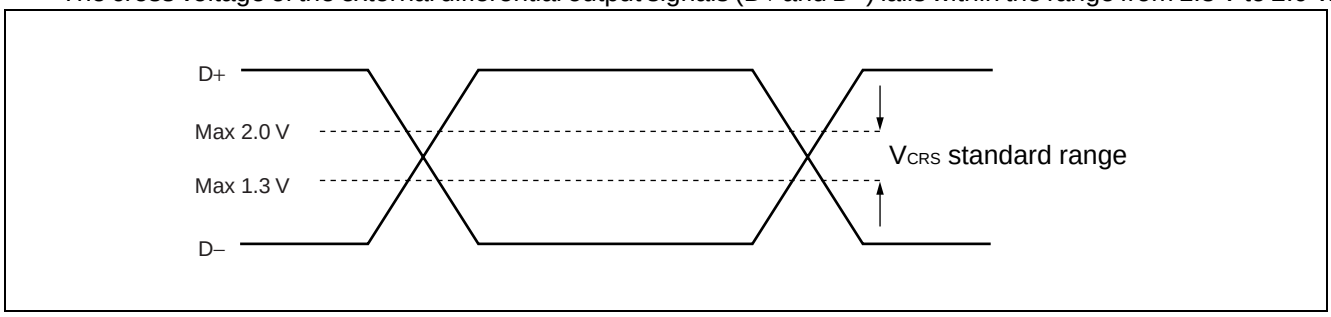
*2 : <Input Levels V_{DI}, V_{CM}>
A differential receiver is used to receive USB differential data signals.
The differential receiver has a differential input sensitivity of 200 mV when the differential data input falls within the range from 0.8 V to 2.5 V with respect to the local ground reference level.

The above voltage range is referred to as common-mode input voltage range.



*3 : <Output Levels V_{OL}, V_{OH}>
The output driving performance levels of the driver are 0.3 V or less (to 3.6-V, 1.5 kΩ load) in the low state (V_{OL}) and 2.8 V or more (to ground, 1.5 kΩ load) in the high state (V_{OH}) .

*4 : <Output Levels V_{CRS}>
The cross voltage of the external differential output signals (D+ and D–) falls within the range from 1.3 V to 2.0 V.

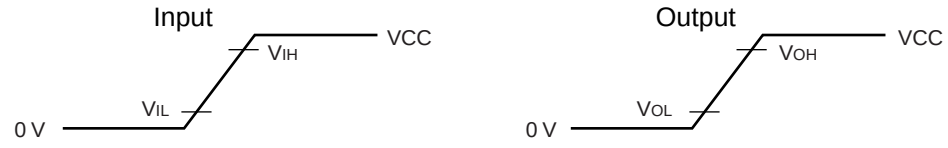


*5 : <Terminations V_{TERM}>
V_{TERM} indicates the pull-up voltage at the upstream port.

4. AC Characteristics

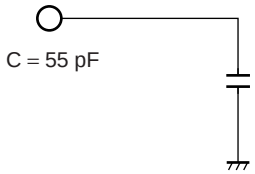
The following measurement conditions depending on the supply voltage apply to the MB91401 unless otherwise specified.

- AC measurement condition



V_{IH}	$V_{DDE} \times 0.8$	V_{OH}	$V_{DDE}/2$
V_{IL}	$V_{DDE} \times 0.2$	V_{OL}	$V_{DDE}/2$

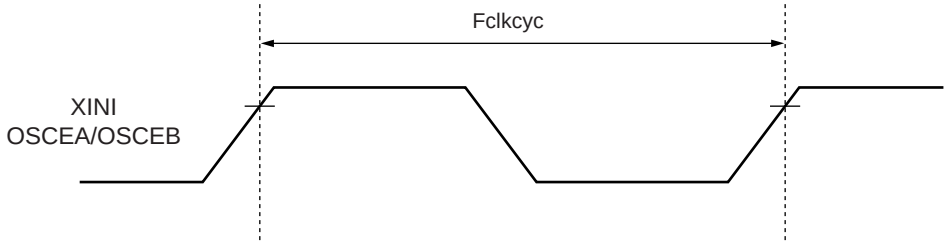
- Load condition



(1) Clock

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
Input clock frequency	Fclkcyc	XINI	External clock	10.0	50.0	MHz	
	Fclkcyc	OSCEA, OSCEB	Oscillation	10.0	50.0	MHz	
Internal operating clock frequency (FR70E/peripheral module)	Fclkin	—	—	—	50.0	MHz	*
Internal operating clock frequency (USBC)	Fusop	—	—	—	48.0	MHz	
Internal operating clock frequency (I^2C IF)	Fi2op	—	—	—	12.5	MHz	
External memory clock frequency	—	MCLKO	—	—	50.0	MHz	

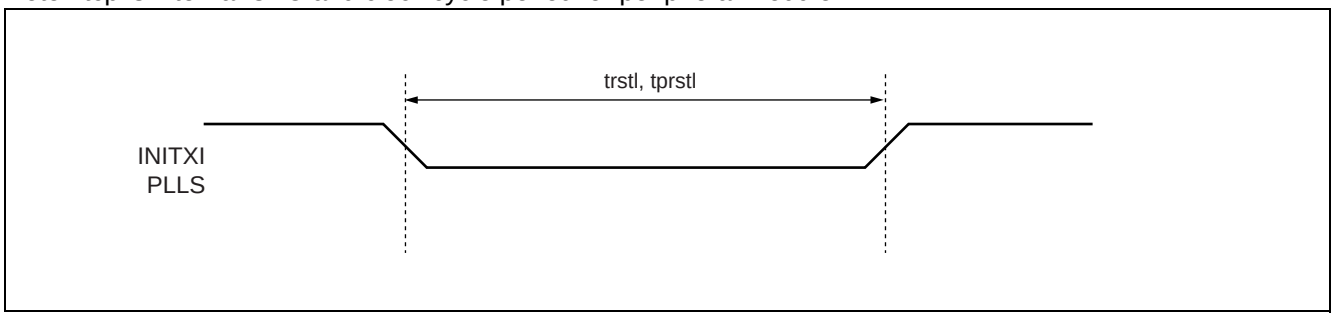
* : The clock frequency must be set to over 25 MHz for the Ethernet MAC interface to perform 100 Base communication.



(2) Reset

Parameter	Symbol	Pin	Conditions		Value		Unit	Remarks
					Min	Max		
Reset input time	trstl	INITXI	After power supply & input clock stabilization	At unusing of PLL	5 tcp	—	ns	
				At using of PLL	600 + 1	—	µs	
PLL reset input time	tprstl	PLLS		At using of PLL	1	—	µs	

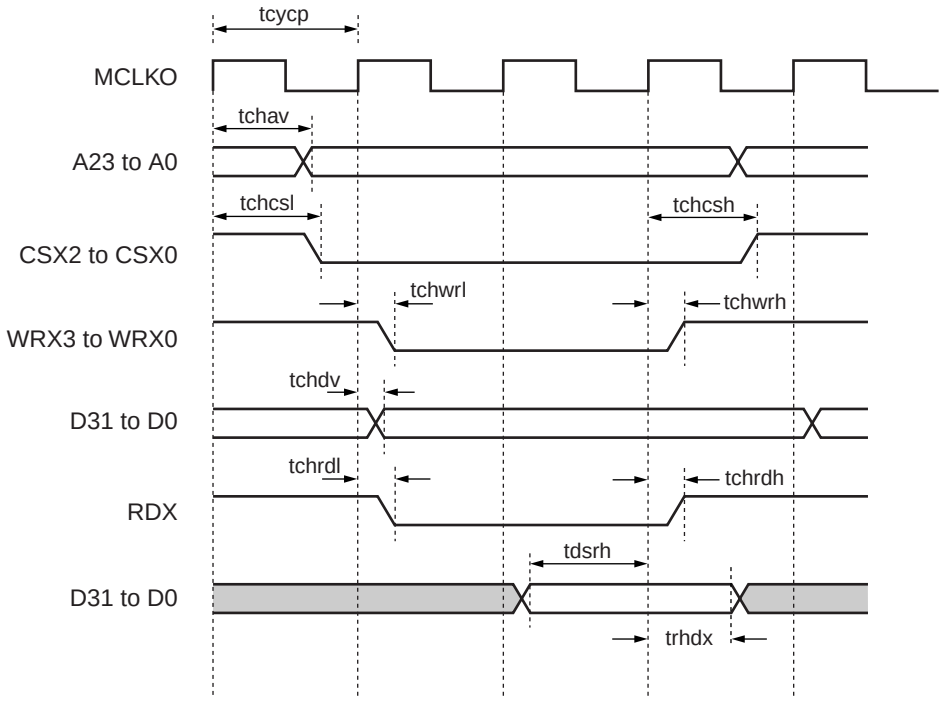
Note : tcp is internal CPU and clock cycle period for peripheral module.



(3) Normal memory access

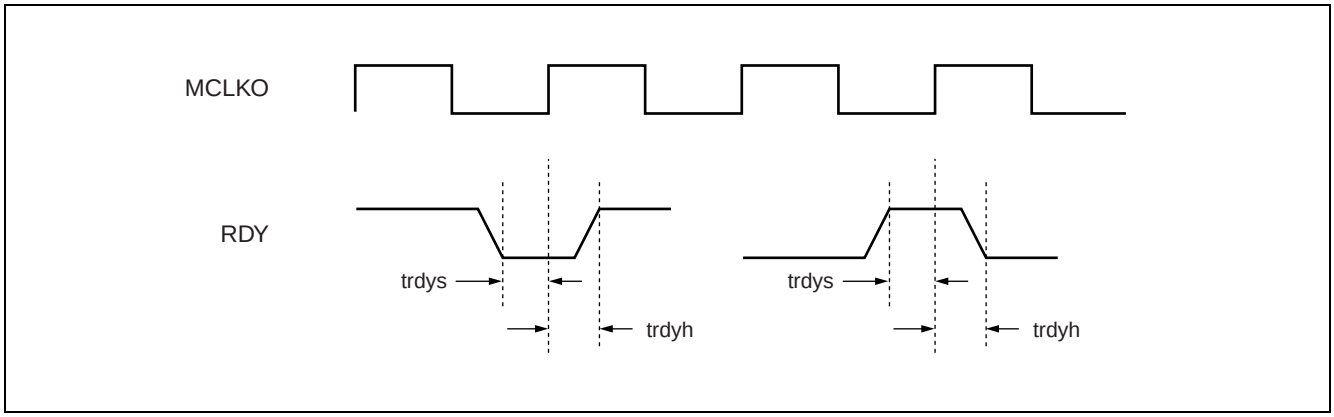
Parameter	Symbol	Pin	Typical timing	Value		Unit	Remarks
				Min	Max		
Address delay time	tchav	A23 to A0	MCLKO ↑	0	tcycp / 2 + 7	ns	
CSX delay time	tchcsl	CSX2 to CSX0	MCLKO ↑	0	tcycp / 2 + 7	ns	
CSX delay time	tchcsh	CSX2 to CSX0	MCLKO ↑	0	tcycp / 2 + 7	ns	
WRX delay time	tchwrl	WRX3 to WRX0	MCLKO ↑	– 1	9	ns	
WRX delay time	tchwrh	WRX3 to WRX0	MCLKO ↑	– 1	9	ns	
Data delay time	tchdv	D31 to D0	MCLKO ↑	0	tcycp / 2 + 7	ns	
RDX delay time	tchrdl	RDX	MCLKO ↑	– 1	9	ns	
RDX delay time	tchrdh	RDX	MCLKO ↑	– 1	9	ns	
Data setup	tdsrh	D31 to D0	MCLKO ↑	19	—	ns	
Data hold	trhdx	D31 to D0	MCLKO ↑	– 1	—	ns	

Note : tcycp is external memory clock cycle period.



(4) Ready input

Parameter	Symbol	Pin	Typical timing	Value		Unit	Remarks
				Min	Max		
RDY setup	trdys	RDY	MCLKO ↑	19	—	ns	
RDY hold	trdyh	RDY	MCLKO ↑	– 1	—	ns	

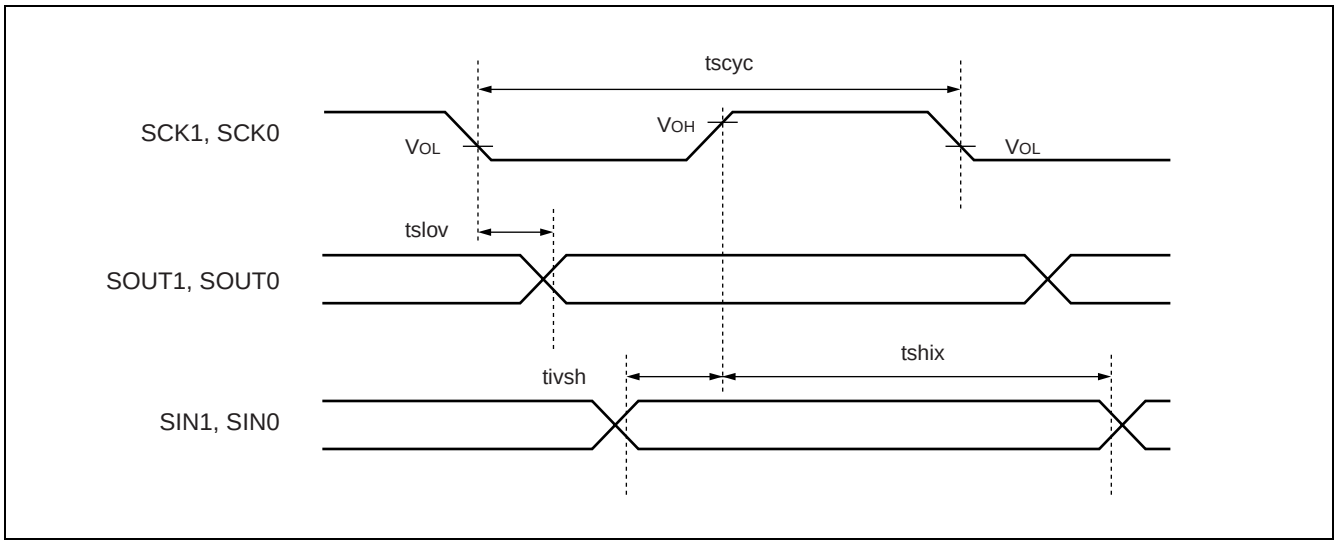


(5) UART

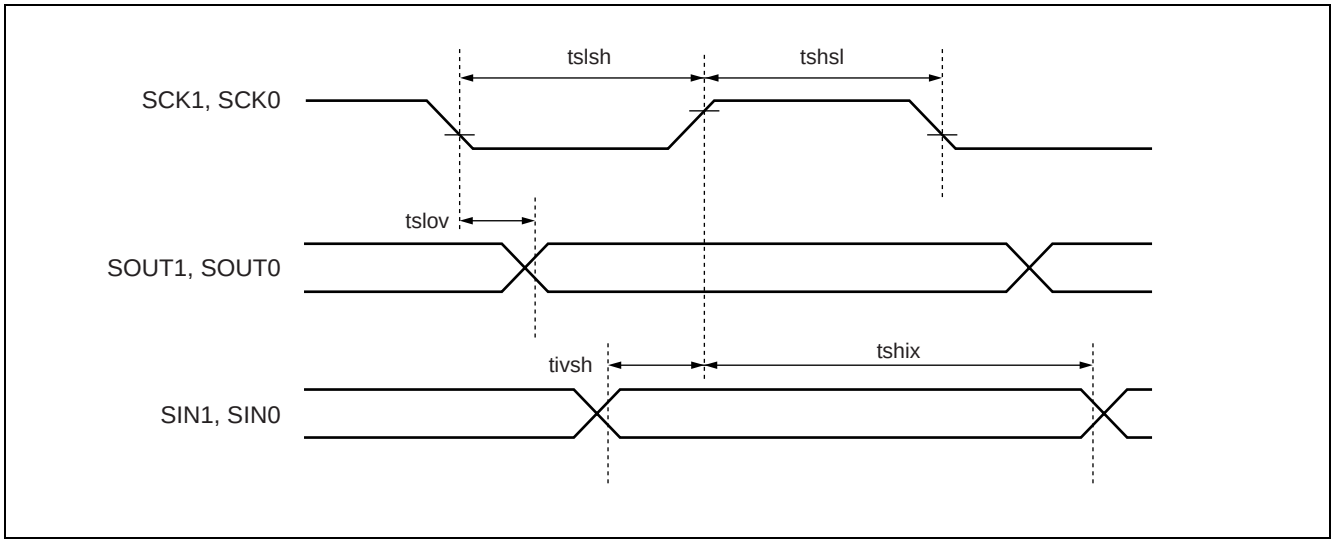
Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	tscyc	SCK1, SCK0	Internal shift clock mode	8 × timcycp	—	ns	
SCLK ↓ → SOUT delay time	tslov	SOUT1, SOUT0		− 80	80	ns	
Valid SIN → SCLK ↑	tivsh	SIN1, SIN0		100	—	ns	
SCLK ↑ → valid SIN hold time	tshix	SIN1, SIN0		60	—	ns	
Serial clock “H” Pulse Width	tshsl	SCK1, SCK0	External shift clock mode	4 × timcycp	—	ns	
Serial clock “L” Pulse Width	tslsh	SCK1, SCK0		4 × timcycp	—	ns	
SCLK ↓ → SOUT delay time	tslov	SOUT1, SOUT0		—	150	ns	
Valid SIN → SCLK ↑	tivsh	SIN1, SIN0		60	—	ns	
SCLK ↑ → valid SIN hold time	tshix	SIN1, SIN0		60	—	ns	

Note : timcycp is operational clock period of peripheral module built-in FR70E core.

• Internal shift clock mode



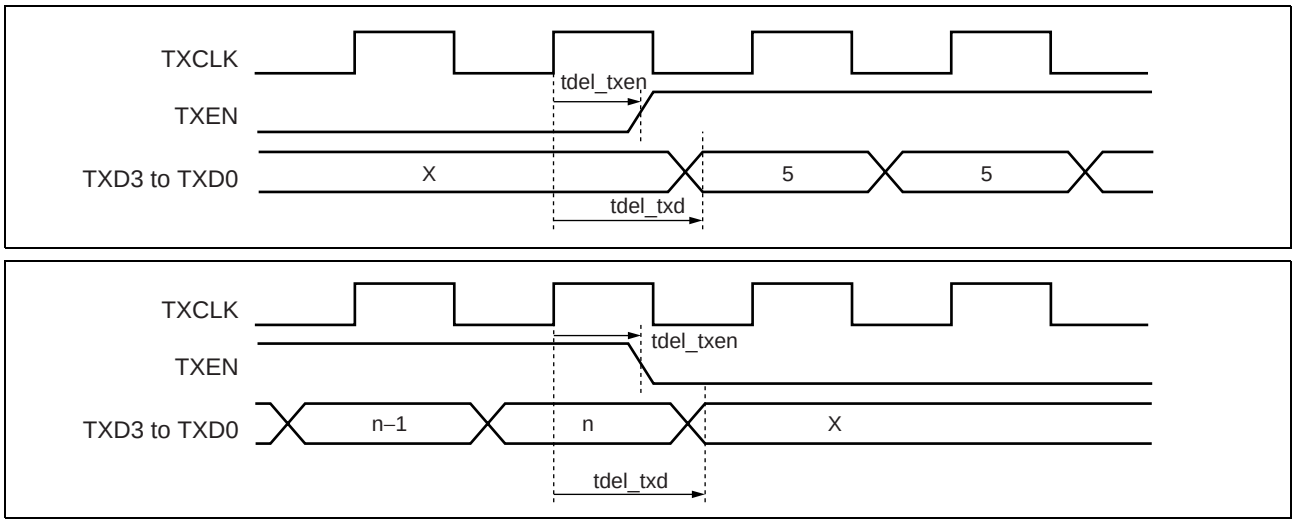
• External shift clock mode



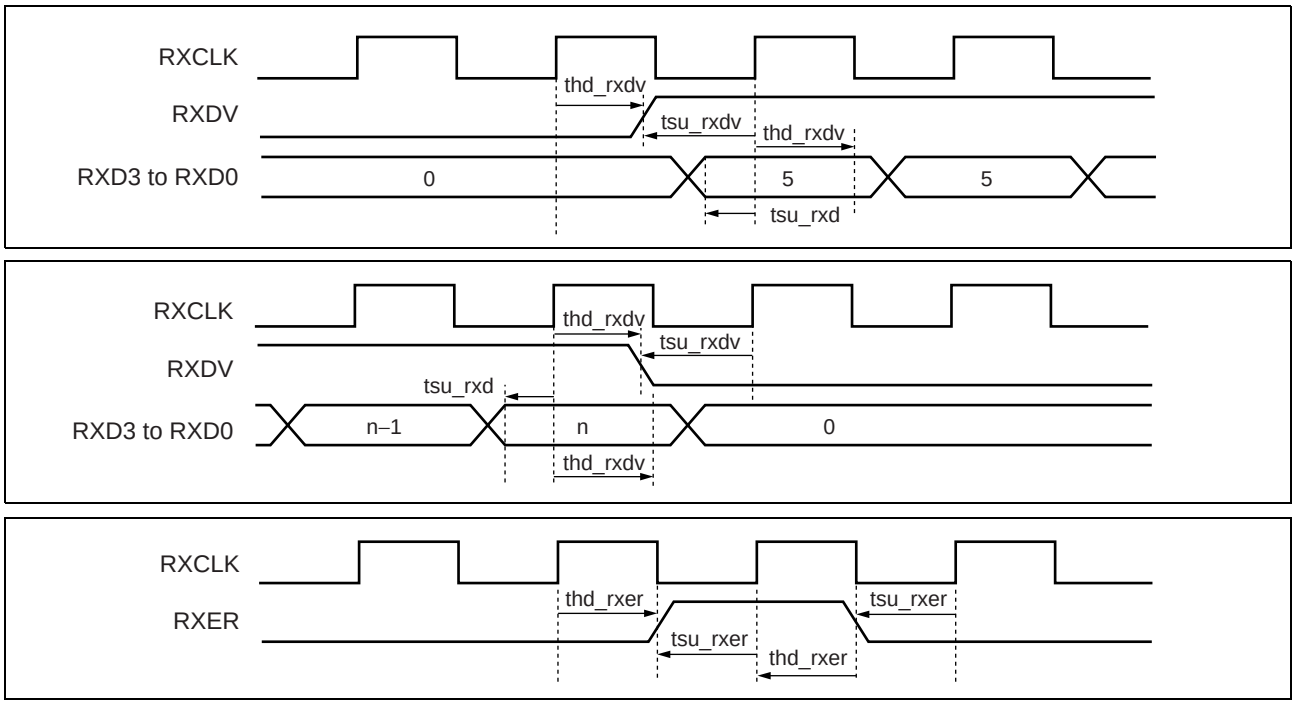
(6) MII interface

Parameter	Symbol	Pin	Typical timing	Value		Unit	Remarks
				Min	Max		
TXEN delay time	tdel_txen	TXEN	TXCLK ↑	0	15	ns	
TXD delay time	tdel_txd	TXD3 to TXD0	TXCLK ↑	0	15	ns	
RXDV setup time	tsu_rxdv	RXDV	RXCLK ↑	2	—	ns	
RXSV Hold Time	thd_rxdv	RXDV	RXCLK ↑	3	—	ns	
RXD setup time	tsu_rxd	RXD3 to RXD0	RXCLK ↑	2	—	ns	
RXD Hold Time	thd_rxdv	RXD3 to RXD0	RXCLK ↑	3	—	ns	
RXERsetup time	tsu_rxer	RXER	RXCLK ↑	2	—	ns	
RXER Hold Time	thd_rxer	RXER	RXCLK ↑	3	—	ns	

• Transmission

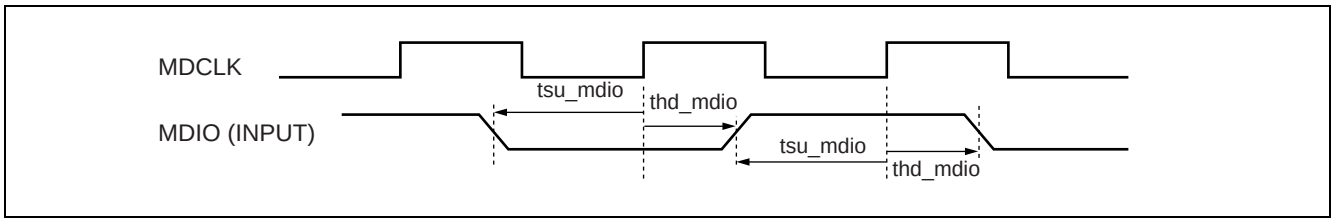


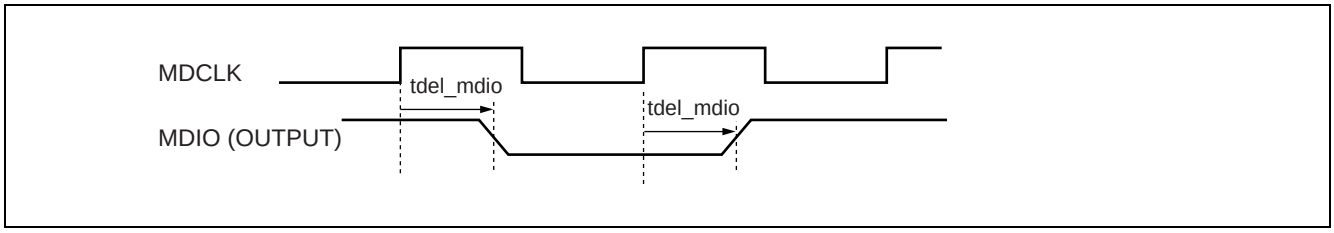
• Reception

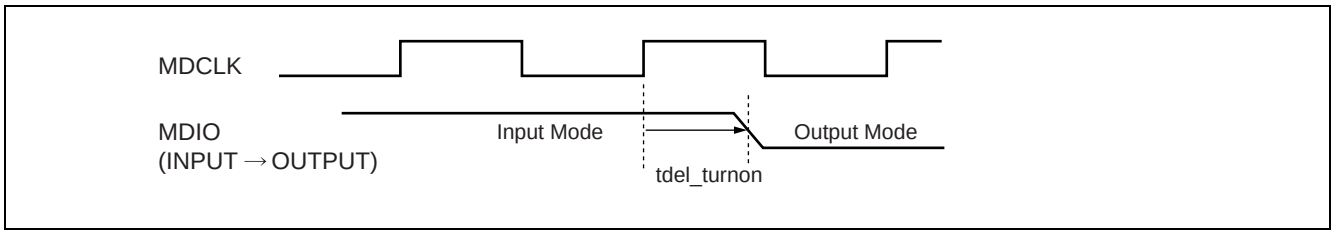


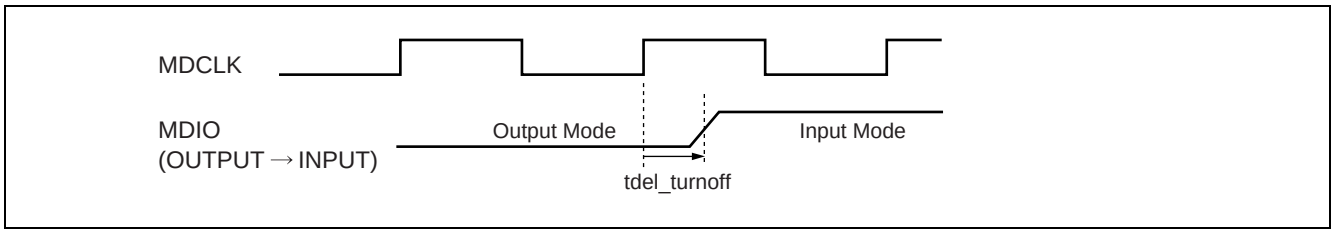
(7) MDIO interface

Parameter	Symbol	Pin	typical timing	Value		Unit	Remarks
				Min	Max		
MDIO setup time	tsu_mdio	MDIO	MDCLK ↑	10	—	ns	
MDIO Hold Time	thd_mdio	MDIO	MDCLK ↑	0	—	ns	
MDIO delay time	tdel_mdio	MDIO	MDCLK ↑	10	30	ns	
MDIO switching time (IN → OUT)	tdel_turnon	MDIO	MDCLK ↑	10	30	ns	
MDIO switching time (OUT → IN)	tdel_turnoff	MDIO	MDCLK ↑	10	30	ns	







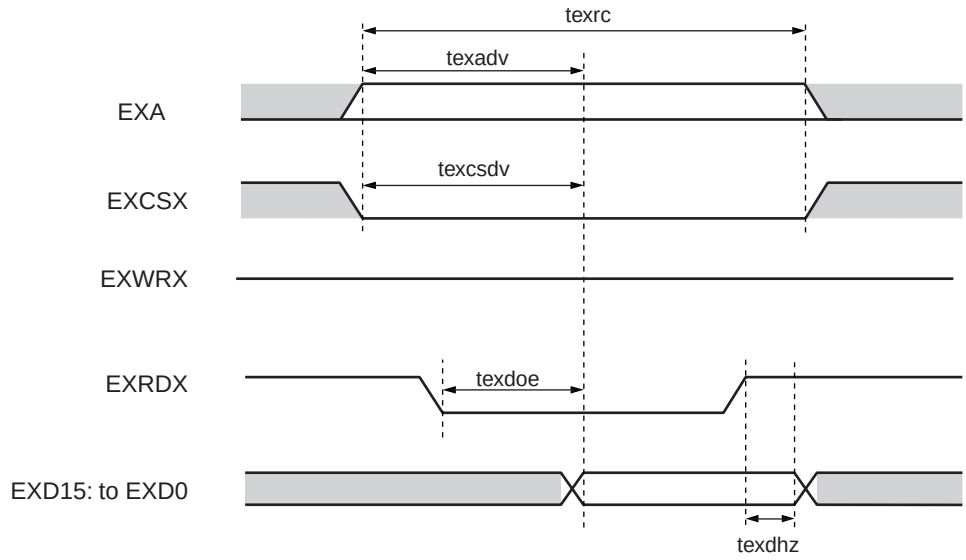


(8) External IF

• Read access

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
EX Read Cycle time	texrc	EXA, EXCSX	6 × tcp	—	ns	
EXA to Data Valid	texadv	EXA, EXD	5 × tcp	—	ns	
EXCSX to Data Valid	texcsdv	EXCSX, EXD	5 × tcp	—	ns	
EXRDX to Data Out Enable	texdoe	EXRDX, EXD	5 × tcp	—	ns	
EXRDX “H” to High Z	texdhz	EXRDX, EXD	—	5 × tcp + 8	ns	

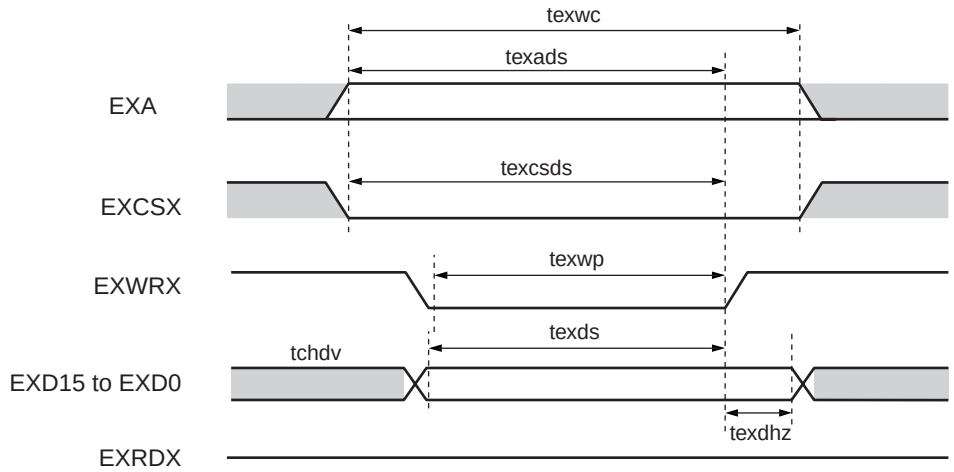
Note : tcp is internal CPU and operational clock period for peripheral module.



• Write access

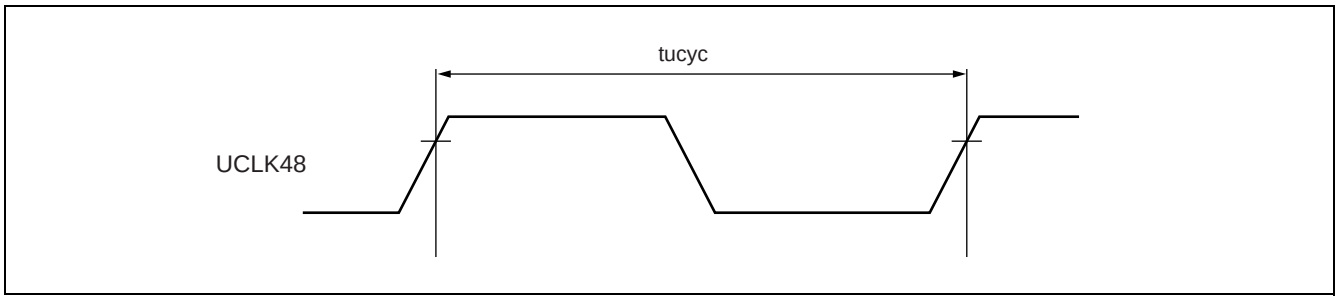
Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
EX Write Cycle time	texwc	EXA, EXCSX	5 × tcp	—	ns	
EXA to Data Setup time	texads	EXA, EXD	4 × tcp	—	ns	
EXCSX to Data Setup time	texcsds	EXCSX, EXD	4 × tcp	—	ns	
EXWRX “L” Pulse width	texwp	EXRDX, EXD	4 × tcp	—	ns	
EXD Setup time	texds	EXRDX, EXD	11	—	ns	
EXD Hold time	texdh	EXRDX, EXD	0	—	ns	

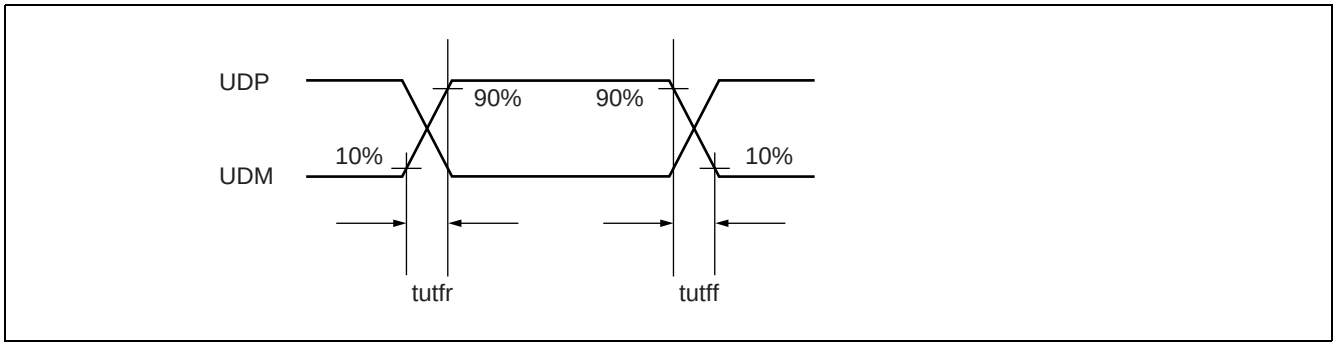
Note : tcp is internal CPU and operational clock period for peripheral module.



(9) USB interface

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Input clock	tucyc	UCLK48	—	48*1	—	MHz	2500ppm accuracy*1
RISE Time	tutfr	UDP, UDM	4	—	20	ns	*2
Fall Time	tutff	UDP, UDM	4	—	20	ns	*2
Differential Rise and Fall Timing Matching	tutfrfm	UDP, UDM	90	—	111.11	%	*2
Driver Output Resistance	tzdrv	UDP, UDM	28	—	44	Ω	*3

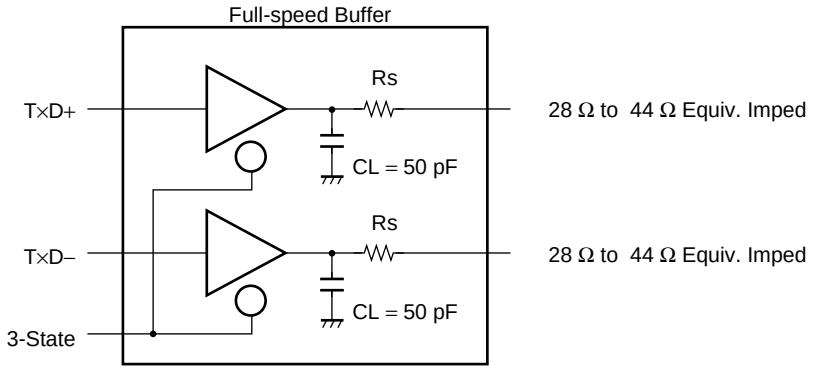




*1 : The AC characteristics of the USB interface conform to USB Specification Revision 1.1.

*2 : <Driver Characteristics TFR, TFF, TFRFM>
These items specify the differential data signal rise (trise) and fall (tfall) times.
These are defined as the times between 10% to 90% of the output signal voltage.
For the full-speed buffer, trise and tfall are specified such that the tr/tf ratio falls within ± 10% to minimize RFI radiation.

*3 : <Driver Characteristics ZDRV>
USB full-speed connection is performed via a shielded twisted-pair cable at a characteristic impedance of 90 Ω ± 15%. The USB Standard stipulates that the USB driver's output impedance must be within the range of 28 Ω to 44Ω. The USB Standard also stipulates that a discrete serial resistor (R_S) must be added to have balance while satisfying the above standard.
The output impedance of the USB I/O buffer on this LSI is about 3 Ω to 19 Ω. Serial resistor R_S to be added must be 25 Ω to 30 Ω (27 Ω recommended) .
Capacitor CL of 50 pF must be added as well.



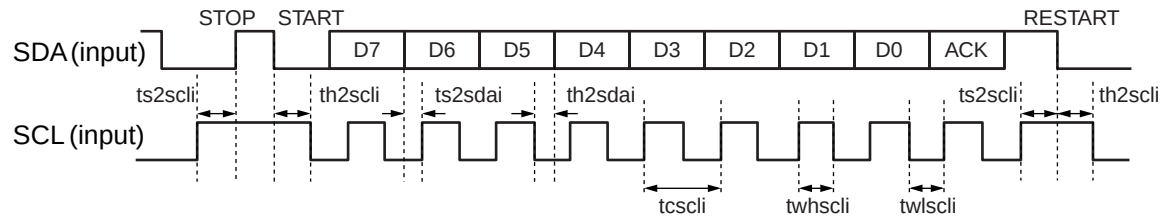
Notes :
- Driver output impedance 3 Ω to 19 Ω
- Rs series resistance: 25 Ω to 30 Ω
- Add a series resistor of preferably 27 Ω

(10) I²C interface

• Input timing specification

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
SDA input setup time	ts2sdai	SDA	250	—	ns	*
SDA input hold time	th2sdai	SDA	0	—	ns	*
SCL cycle time	tcscli	SCL	10	—	µs	*
SCL input “H” pulse time	twhscli	SCL	4	—	µs	*
SCL input “L” pulse time	twlscli	SCL	4.7	—	µs	*
SCL input setup time	ts2scli	SCL	4	—	µs	*
SCL input hold time	th2scli	SCL	4.7	—	µs	*

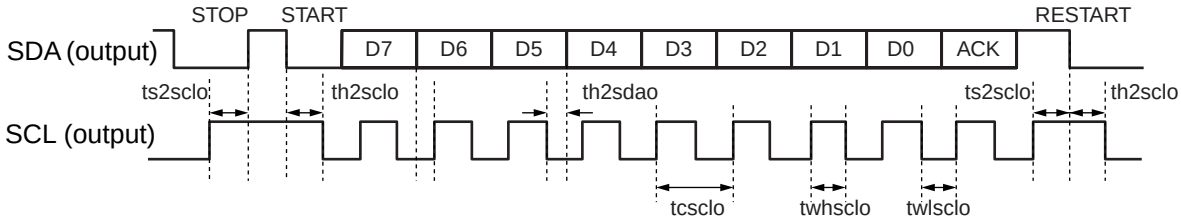
* : Initial Value : I²C bus standards.



• Output timing specification

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
SCL output cycle time	tcsclo	SCL	$(2 \times m) + 2$	—	PCLK	*
SCL output “H” Pulse Time	twhsclo	SCL	$m + 2$	—	PCLK	*
SCL output “L” Pulse Time	twlsclo	SCL	m	—	PCLK	*
SCL output setup time	ts2sclo	SCL	$m + 2$	—	PCLK	*
SCL output hold time	th2sclo	SCL	$m \times 2$	—	PCLK	*
SDA output hold time	th2sdao	SDA	5	—	PCLK	*

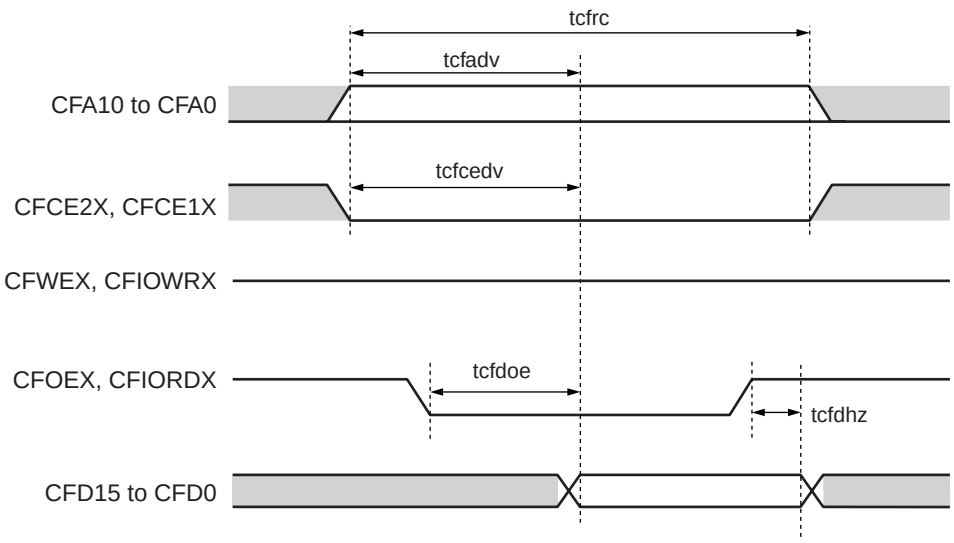
* : For value m, refer to Section 7.5.2.3 “Clock Control Register (CCR) in the I²C Interface Specifications.” PCLK indicates I²C interface operating clock frequency.



(11) Card IF

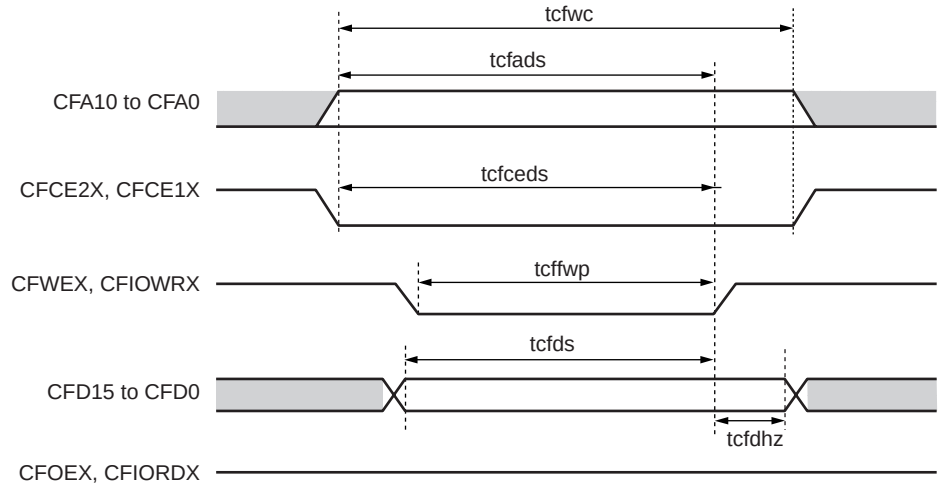
• Read access

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
CF Read Cycle time	tcfrc	CFA10 to CFA0, CFCE2X, CFCE1X	—	—	ns	
CFA to Data Valid	tcfadv	CFA10 to CFA0, CFD15 to CFD0	—	—	ns	
CFCEX to Data Valid	tcfcedv	CFCE2X, CFCE1X, CFD15 to CFD0	—	—	ns	
CFOEX CFIORDX to Data Out Enable	tcfdoe	CFOEX, CFIORDX, CFD15 to CFD0	—	—	ns	
CFOEX CFIORDX “H” to High Z	tcfdhz	CFOEX, CFIORDX, CFD15 to CFD0	—	—	ns	



• Write access

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
CF Write Cycle time	tcfwc	CFA10 to CFA0, CFCE2X, CFCE1X	—	—	ns	
CFA to Data Setup time	tcfads	CFA10 to CFA0, CFD15 to CFD0	—	—	ns	
CFCEX to Data Setup time	tcfceds	CFCE2X, CFCE1X, CFD15 to CFD0	—	—	ns	
CFWEX CFIOWRX “L” Pulse width	tcffwp	CFWEX, CFIOWRX	—	—	ns	
CFD Setup time	tcfds	CDWEX, CFIOWRX, CFD15 to CFD0	—	—	ns	
CFD Hold time	tcfdhz	CDWEX, CFIOWRX, CFD15 to CFD0	—	—	ns	



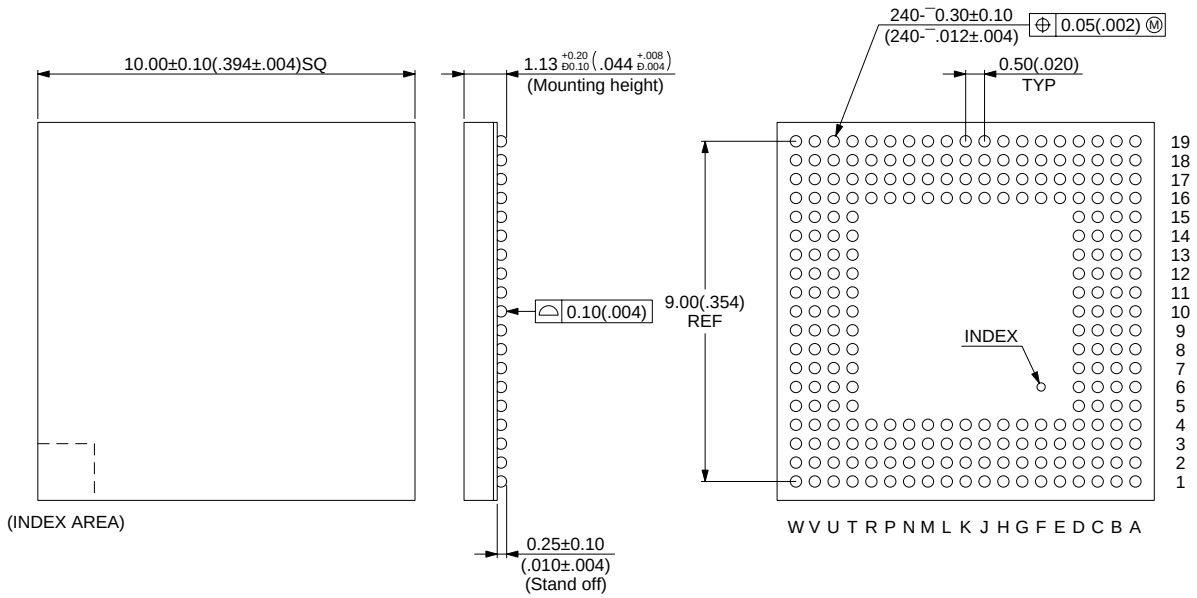
■ ORDERING INFORMATION

Part number	Package	Remarks
MB91401	240-pin plastic FBGA (BGA-240P-M01)	

■ PACKAGE DIMENSION

240-pin plastic FBGA
(BGA-240P-M01)

Note: The actual shape of coners may differ from the dimension.



Dimensions in mm (inches).
Note : The values in parentheses are reference values.

MEMO

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